SPB105-WiFi 802.11b+g Evaluation Kit

# Data Sheet

## SPB105

## WiFi Evaluation Kit

H&D Wireless

Revision History

| Revision | Revision date | Description |
|---|---|---|
| **PA1** | 2009-10-14 | First issue |
| **PA2** | 2009-11-09 | Second Draft |
| **PA3** | 2009-11-13 | Final draft for review |
| **A** | 2009-11-15 | First release |
| **B** | 2009-12-18 | Certification data, new address |
| **PC1** | 2010-01-25 | Updated for new revision |
| **C** | 2010-02-22 | Release after review |
| **PD1** | 2010-02-25 | Reference schematic update |
| **D** | 2010-03-17 | FCC number updated |
| **PE1** | 2010-04-14 | RF Interface clarified |
| **PE2** | 2010-04-26 | SDIO SPI interface updated |

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# 1 INTRODUCTION

## 1.1 Overview

SPB105 is an evaluation kit for the HDG104 WLAN System In Package, SIP module. It is a complete solution designed to be plugged in to the WLESS header on Atmel EVK1104 and EVK1105 AVR32 MCU evaluation kits.
It can also be used as a component for any host system needing a complete wifi solution.

SPB105 enables a cost efficient ultra low power, high performance and feature rich client solution. It provides up to 54 Mbit/s data rate when operating in the OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.

The host interface supports SPI communication when used in the 10-pin RF-header connection (WLESS) and SDIO when used in a custom board with the AVR32UC3A3, and software drivers and a complete application example is included in Atmel AVR32 UC3B Software Framework from version 1.5.0 and onwards.

## 1.2 Key Features

- Data Rates: 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54Mbps
- Modulation: QPSK, 16QAM, 64QAM DBPSK, DQPSK, CCK, OFDM with BPSK
- WEP and AES hardware encryption accelerator up to 128 bits
- Chip Antenna and connector for external antenna (optional) mounted on the board.
- Low power consumption due to efficient class AB PA design
- UMA Compliant
- Advanced power management for optimum power consumption at varying load.
- Bluetooth Coexistence support
- Power Supply 3.3 V from EVK board
- Small footprint 24x40 mm
- RoHS Compliant

# 2 HARDWARE ARCHITECTURE

## 2.1 Block Diagram

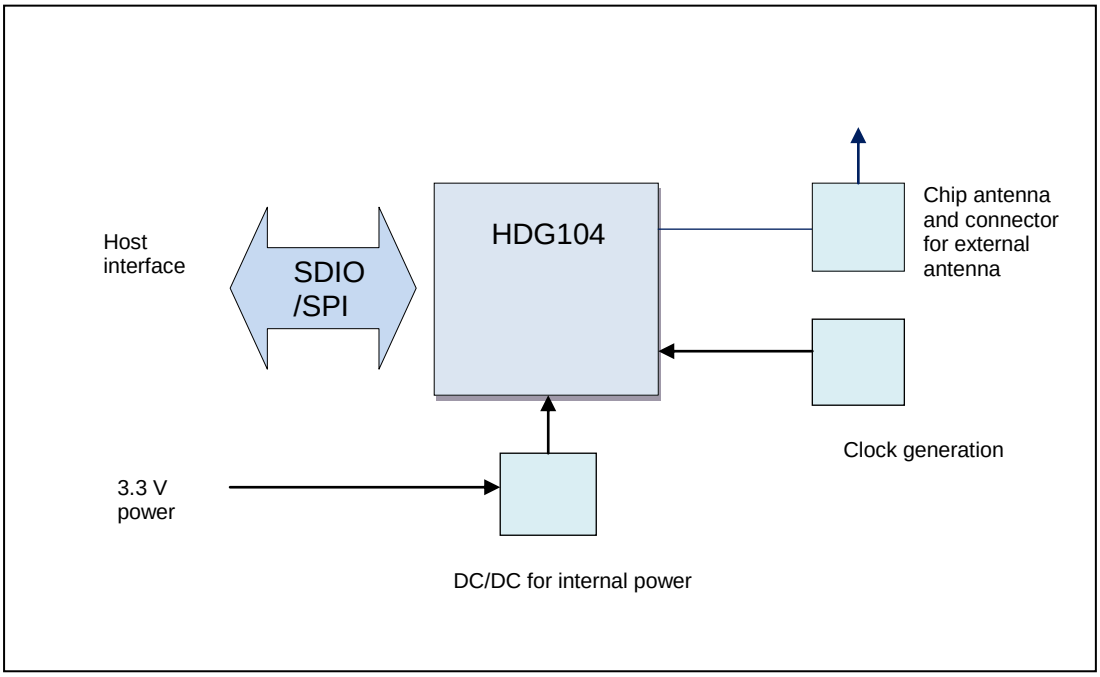



*Figure 2.1: Block diagram.*

## 2.2 Order information

.

| Part No. | option | Batch size | Shipment package |
|---|---|---|---|
| SPB105/1 | | 10/100 | Unit in ESD bag |
| SPB105/3 | | 1K/10K/50K | Tray |
| SPB105/e/3 | Ext antenna connector not mounted. | 1K/10K/50K | Tray |

*Table 2.2: Order information.*

# 3 ELECTRICAL DATA

## 3.1 Absolute maximum ratings

| Rating | Min | Max | Unit |
|---|---|---|---|
| Supply voltage | 0 | 4 | V |
| Input RF level | | 10 | dBm |
| Storage temperature | -50 | +125 | $^{o}$C |

*Table 3.1: Abolute maximum ratings. Exceeding any of the maximum ratings, even briefly lead to deterioration in performance or even destruction. Values indicates condition applied one at the time.*

## 3.2 ESD

HDG104 withstands ESD voltages up to 2000 V tested with HBM (Human Body Model) according to JESD22-A114 and up to 300 V tested with MM (Machine Model) according to JESD22-A115.

## 3.3 Recommended operating conditions

| Rating | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply Voltage VCC | 2.75 | 3.3 | 3.6 | V |
| Operating temperature | -20 | +25 | +70 | $^{o}$C |
| Operating temperature, reduced spec, no damage. | -30 | +25 | +85 | $^{o}$C |

*Table 3.3: Recommended operating conditions*

## 3.4 Power Consumption

### 3.4.1 Current Consumption

| Mode | Conditions | Parameter | Voltage | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **All modes** | | VBAT_P+VCC+ VPA+VBAT_32K | 3.6 V | | | 250 | mA |
| **All modes** | | VPA | 3.6 V | | | 150 | mA |
| **All modes** | | VBAT_P+VCC | 3.6 V | | | 150 | mA |
| **All modes** | | DVDD | 1.2 V | | | 100 | mA |
| **All modes** | 25ºC | VBAT_32K | 3.3 V | | 10 | | µA |
| **Tx** | 25ºC | DVDD | 1.2 V | | 15 | | mA |
| **Rx** | 25ºC | DVDD | 1.2 V | | 60 | | mA |
| **Sleep** | 25ºC | VBAT_P+VCC+ VPA+VBAT_32K | 3.3 V | | 30 | | µA |
| **Sleep** | 25ºC | DVDD | 1.2 V | | 110 | | µA |
| **Soft Shutdown** | 25ºC | VBAT_P+VCC+ VPA+VBAT_32K | 3.3 V | | 20 | | µA |
| **Soft Shutdown** | 25ºC | DVDD | 1.2V | | 70 | | µA |
| **Shutdown,** | 25ºC DVDD OFF | VBAT_P+VCC+ VPA+VBAT_32K | 3.3 V | | 15 | | µA |

*Table 3.4.1: Current consumption in different modes.*

### 3.4.2 Power Consumption

$T_{amb}$=25°C, VCC=VBAT_P=VBAT_32K=VPA=3.3 V, DVDD =1.2 V

| Mode | OutputPower | Power Consumption | Comments |
|---|---|---|---|
| **TX 802.11b** | +17 dBm | 725 mW | 1, 2, 5.5, 11 Mbit/s |
| **TX 802.11g** | +14 dBm | 590mW | 6, 9, 12, 18, 24, 36, 48, 54 Mbit/s |
| **RX 802.11b** | N/A | 220mW | |
| **RX 802.11g** | N/A | 230mW | |
| **Power Save** | N/A | 0,4 mW | Receive only, 2s RX beacons |
| **Sleep** | N/A | 0,2mW | No receive, FW loaded, only LFC running |
| **Soft Shutdown** | N/A | 0,15 mW | No receive, No FW loaded, only LFC running |
| **Shutdown** | N/A | 0,05 mW | No FW loaded, DVDD OFF, |

*Table 3.4: Power consumption in different modes.*

## 3.5 RF Performance

VCC=VPA= 2.75 – 3.6V, DVDD=1.15 - 1.25V External supply, Tamb= -20 – +70°C

| Parameter | Conditions | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| **Frequency range** | | 2400 | | 2500 | MHz |
| **RF impedance** | | | 50 | | ohm |
| ***Transmitter performance*** | | | | | |
| **Output power** | QPSK, Calibrated. | +16,5 | +17 | +17,5 | dBm |
| **Output power** | OFDM 54Mbit/s, Calibrated. | +13,5 | +14 | +14,5 | dBm |
| **EVM at +15dBm** | QPSK | | 30 | 35 | % |
| **EVM at +11dBm** | OFDM 54MBit/s | | 3.5 | 5 | % |
| ***Receiver performance*** | | | | | |
| **Receiver sensitivity** | DPSK 1Mbit/s | | -96 | | dBm |
| **Receiver sensitivity** | QDPSK 2Mbit/s | | -92 | | dBm |
| **Receiver sensitivity** | CCK/DPSK 5.5Mbit/s | | -91 | | dBm |
| **Receiver sensitivity** | CCK/BPSKK 11Mbit/s | | -88 | | dBm |
| **Receiver sensitivity** | OFDM 6Mbit/s | | -91 | | dBm |
| **Receiver sensitivity** | OFDM 9Mbit/s | | -90 | | dBm |
| **Receiver sensitivity** | OFDM 12Mbit/s | | -88 | | dBm |
| **Receiver sensitivity** | OFDM 18Mbit/s | | -86 | | dBm |
| **Receiver sensitivity** | OFDM 24Mbit/s | | -83 | | dBm |
| **Receiver sensitivity** | OFDM 36Mbit/s | | -80 | | dBm |
| **Receiver sensitivity** | OFDM 48Mbit/s | | -76 | | dBm |
| **Receiver sensitivity** | OFDM 54Mbit/s | | -74 | | dBm |

*Table 3.5: RF performance.*

## 3.6 Digital pin characteristics

### 3.6.1 SDIO timing characteristics

The SDIO/SPI-interface can run in two different modes, Default mode and High speed mode. SDIO 1-bit default mode is selected at Power On Reset. The default mode is showed in Fig. 3.6.1 and table: 3.6. For the high speed mode see Fig. 3.2 and table: 3.7. Condition: VDDIO= 1.7 – 3.6 V, TA= -20 – +70°C

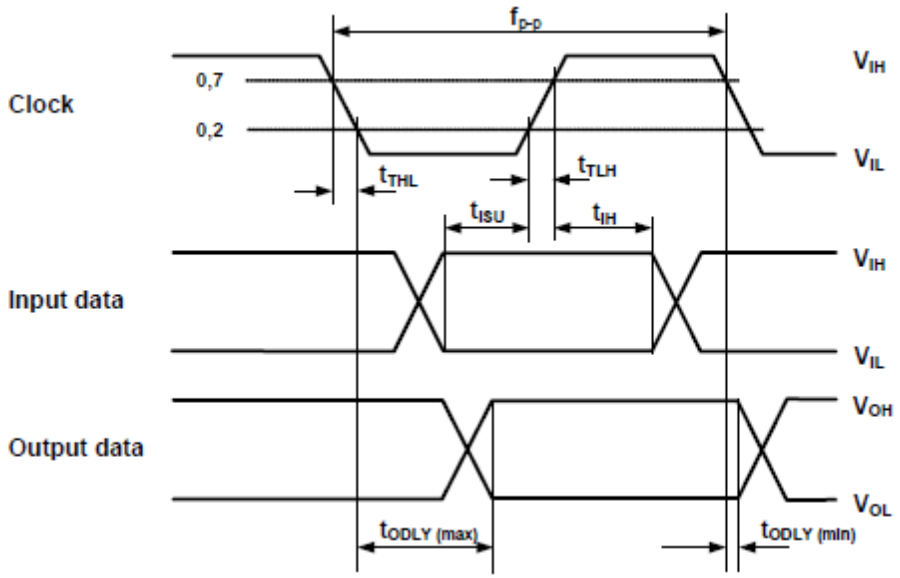



*Figure 3.1: SDIO/SPI timing diagram (default mode)*

| Parameter | Symbol | Min | Max | ns | Comments |
|---|---|---|---|---|---|
| **Input set-up time** | tISU | 5 | | ns | |
| **Input hold time** | tIH | 5 | | ns | |
| **Clock fall time** | tTHL | | 10 | ns | |
| **Clock rise time** | tTLH | | 10 | ns | |
| **Output delay time** | tODLY | 0 | 40 | ns | |

*Table 3.6: SDIO timing parameter values (default mode)*

## 3.6.2 SPI timing characteristics

The SPI-interface timing is shown in Fig. 3.1 and Table 3.6
can run in two different modes, Default mode and High speed mode.
SDIO 1-bit default mode is selected at Power On Reset. The default mode is showed in Fig. 3.6.1 and table: 3.6. For the high speed mode see Fig. 3.2 and table: 3.7. Condition: VDDIO= 1.7 – 3.6 V, TA= -20 – +70°C

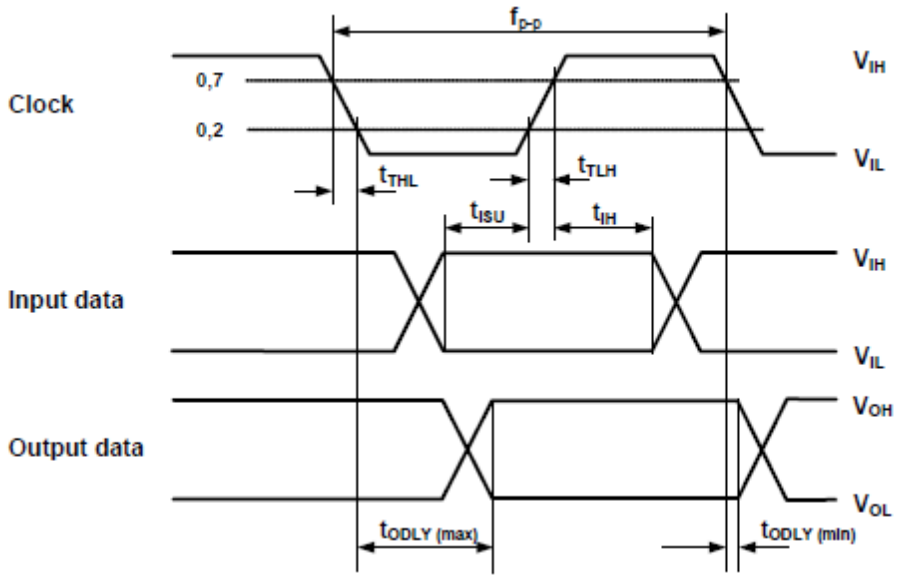



*Figure 3.1: SDIO/SPI timing diagram (default mode)*

| Parameter | Symbol | Min | Max | ns | Comments |
|---|---|---|---|---|---|
| **Input set-up time** | tISU | 5 | | ns | |
| **Input hold time** | tIH | 5 | | ns | |
| **Clock fall time** | tTHL | | 10 | ns | |
| **Clock rise time** | tTLH | | 10 | ns | |
| **Output delay time** | tODLY | 0 | 40 | ns | |

*Table 3.6: SDIO timing parameter values (default mode)*

| Parameter | Symbol | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|---|
| **Input low voltage** | VIL | -0.3 | | 0.2 | V | |
| **Input high voltage** | VIH | 1.5 | | VBAT_32K+0.3 | V | |
| **Input leakage current** | IIL | -1 | | +1 | µA | |
| **Input current** | IIN | | | 2 | mA | During low to high transition |

*Table 3.11: SHUTDOWN pin DC characteristics.*

# 4 PIN CONFIGURATIONS

## 4.1 Standard Pin Configuration

In the standard configuration the SPB105 is delivered with 2x5 pin header, that can be inserted in a female socket, or soldered, on host board. The pin header is mounted with the pins extended down on the bottom side of the board.

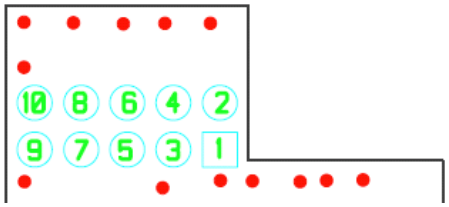



*Figure 4.1: Package pinout top view*

## 4.2 Alternative Pin Configuration

In the alternative configuration an angled female socket is mounted on the top (component) side of the board, angled towards the edge of the board. This is for plugging directly in to the angled pin header on the Atmel EVK1104/1105 evaluation boards. Otherwise the pinout is the same is in the standard configuration (fig 4.1)

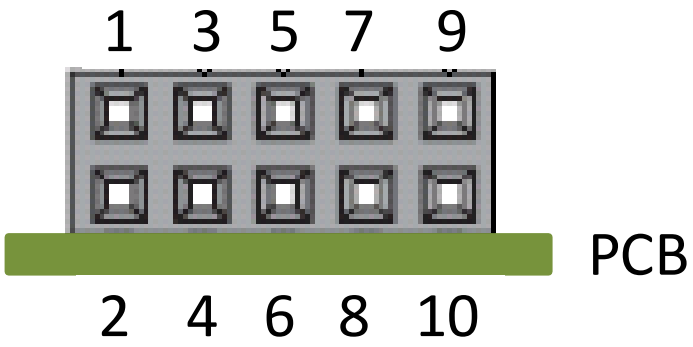



*Figure 4.2: Package pinout. front view*

## 4.3 Pin assignments

| Pin | Function | Type | Description |
|---|---|---|---|
| **1** | SDIO_D2 | I/O | Databit 2 |
| **2** | GPIO | I/O | Not used |
| ***3*** | SDIO_D1/SPI_IRQ | I/O | Databit 1 / Interrupt, GPIO62 |
| **4** | RESET | I | Shutdown, GPIOXX |
| **5** | SDIO_D3/SPI_CS | I/O | Databit 3/ SPI Chip Select |
| **6** | SDIO_CMD / SPI_MOSI | I/O | SDIO_CMD / SPI_MOSI |
| **7** | SDIO_D0/SPI_MISO | I/O | Databit 0 / SPI_MISO |
| **8** | SDIO_CLK/SPI_CLK | I | SPI Clock |
| **9** | GND | S | Ground |
| **10** | VCC | S | Power supply |

*Table 4.1: Pin Description for the board..*

# 5 APPLICATION INFORMATION

## 5.1 Power Supply

SPB105 should be powered by a 3.3V supply. When the SPB105 is used with Atmel EVK1104 and EVK1105 it is supplied by the EVK board.

## 5.2 Reset/Shutdown

The SPB105 is equipped with an onboard reset circuit. Should the supply voltage (VCC) fall below 2.63 V the HDG104 SHUTDOWN pin, active low, is set low and the SPB105 is set in Shutdown mode. When the VCC rises above 2.63 V the RESET pin is set high after 240 us and the HDG104 is set in active mode.

The RESET pin is also available on pin 4 of SPB105. As the signal is actively driven high by the reset circuit it is recommended to disconnect the reset circuit before using external control for RESET signal.

## 5.3 Power save

Power save is a energy saving mode where SPB105 is only listening at regular intervals for the beacons transmitted from an access point and is set in sleep mode in between. During this sleep mode, FW is kept in RAM but all not needed functions are turned off. Since the receive time is very short compared to the listening interval the average current consumption is reduced significantly. The timing of the listening interval is based on the LFC (32 kHz) clock. The LFC is implemented internally.
For detailed information regarding the power save function see the Application manual.

## 5.4 Interfaces

To communicate with the SPB105 the SPI or SDIO interface is used.

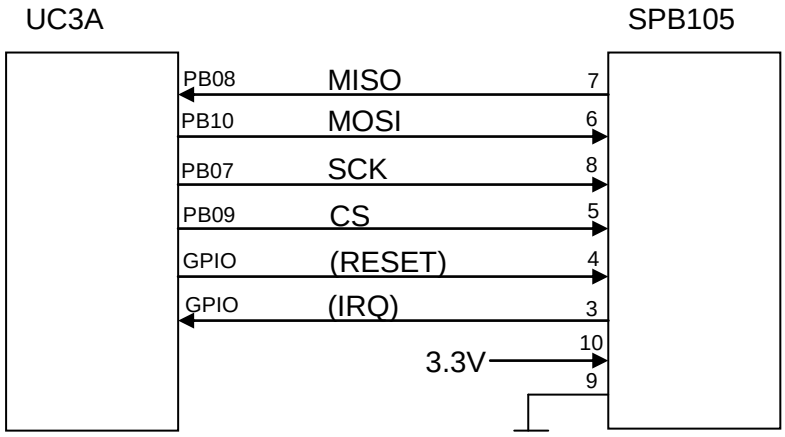
### 5.4.1 SPI interface

The SPI interface signals are connected to the host boards SPI bus. It can coexist with other SPI devices on the same bus. The SPI_CS signal is the Chip Select signal, and it is implemented with a General Purpose I/O pin.

The SPI bus signals on the Atmel AVR32 family processors use different pins for different parts in the family, and depending on the application the processors can be configured to use different pins for SPI. As an example for the UC3A the following configuration can be made:

| Pin | Function | Pin on AVR32 | Description |
|---|---|---|---|
| **1** | - | **-** | Not used |
| **2** | - | - | Not used |

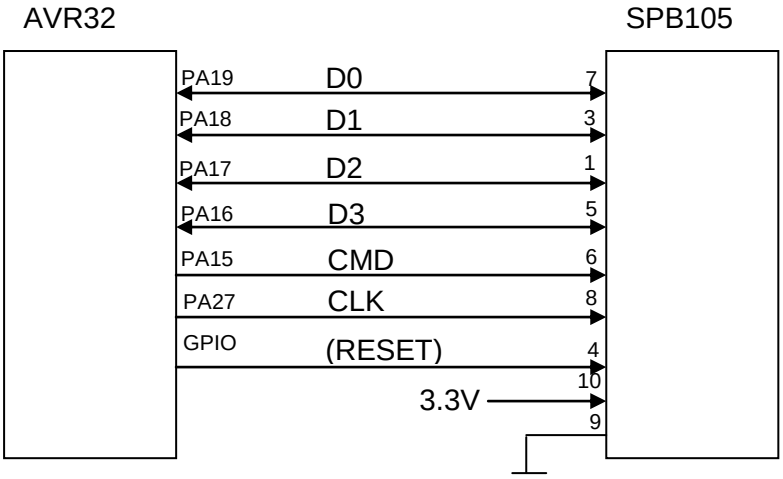
| | | | |
|---|---|---|---|
| ***3*** | SPI_IRQ | GPIO pin, configured to generate interrupt. (optional) | Interrupt |
| **4** | RESET | GPIO pin, put SPB105 in shutdown mode, reset. (optional) | Shutdown |
| **5** | SPI_CS | PB09 (SPI1_NPCS[0]) | SPI Chip Select |
| **6** | SPI_MOSI | PB10 (SPI1 MOSI) | SPI_MOSI |
| **7** | SPI_MISO | PB08 (SPI1 MISO) | SPI_MISO |
| **8** | SPI_CLK | PB07 (SPI1 SCK) | SPI Clock |
| **9** | GND | - | Ground |
| **10** | VCC | - | Power Supply, 3.3V |




### 5.4.2 SDIO interface

For the SDIO interface four GPIO pins are used as data bits, these can be any of the MCI groups available on the AVR32 processor. The SDIO_CMD should be in the same group. The optional RESET can be connected to be any GPIO pin. This is an example of pins to can be used:

| Pin | Function | Pins on AVR32 family processor | Description |
|---|---|---|---|
| **1** | SDIO_D2 | PA17 (MCI – DATA10) | Databit 2 |
| **2** | - | - | Not used |
| ***3*** | SDIO_D1 | PA18 (MCI – DATA9) | Databit 1 |
| **4** | RESET | Any GPIO (optional) | Shutdown |
| **5** | SDIO_D3 | PA16 (MCI – DATA11) | Databit 3 |
| **6** | SDIO_CMD | PA15 (MCI – CMD [1]) | SDIO_CMD |
| **7** | SDIO_D0 | PA19 (MCI – DATA8) | Databit 0 |
| **8** | SD_CLK | PA27 (MCI – CLK) | SDIO Clock |
| **9** | GND | **-** | Ground |
| **10** | VCC | - | Power Supply |




## 5.5 RF interface

The SPB105 has a high performance chip antenna as the primary RF interface. To enable RF measurements a coaxial connector is available. The connector is switching and compatible with MuRata measurement probe MXHS83QH3000 and similar.

## 5.6 General application information

### 5.6.1 Design directions

The design using the SPB105 must be performed according to good RF design considerations. All the leads shall be as short as possible between the circuit pins and the external components.

### 5.6.2 Environmental statement

The SPB105 is designed and manufactured to comply with the RoHS and Green directives.

# 6 PACKAGE SPECIFICATIONS

## 6.1 Mechanical outline of the SPB105 circuit board

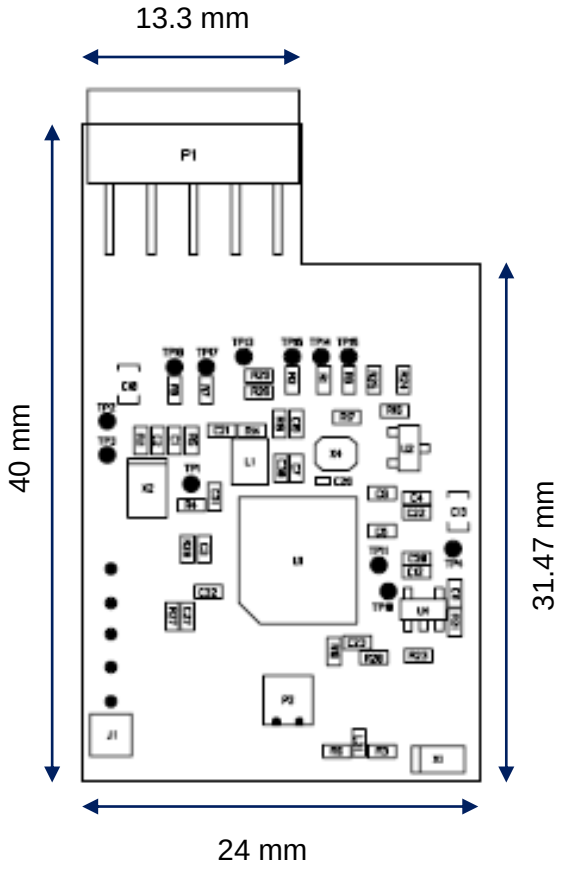



*Figure 6.1: Mechanical drawing.*

## 6.2 Markings on the SPB105

The circuit board are marked with a sticker with the units serial number and FCC id. X02HDG104

# 7 STANDARDS COMPLIANCE

## 7.1 IEEE/IETF

| Standard | Revision | Description |
|---|---|---|
| **802.11** | 802.11 R2003 | WLAN MAC& PHY |
| **802.11b** | 802.11 R2003 | High rate DSSS (5,5/11Mbit/s) |
| **802.11d** | 802.11 R2003 | Operation in different regulatory domains |
| **802.11e** | D9,0 Aug. 2004 | QoS enhancements |
| **802.11g** | -2003 | Extended rate PHY (ERP-PBCC, DSS-OFDM) |
| **802.11i** | -2004 | Security enhancements |
| **802.11k** | Draft 11.0, 2008 | Wireless network management |
| **802.11r** | Draft 9.0, 2008 | Fast BSS transition |
| **802.11h** | 1997 edition | Bridge tunneling |
| **RFC1023** | Inherent | Frame encapsulation |
| **802.15.2** | | Bluetooth coexistence |

***Table** 7.1: applicable IEEE standards*

## 7.2 WiFi

| Specification | Description | Revision |
|---|---|---|
| **Wi-Fi 802.11b with WPA system inter operability test plan for IEEE 802.11b devices** | 802.11b devices with WPA | 2.1 |
| **WiFi 802.11g with WPA system inter operability test plan** | 802.11g devices with WPA | 2.0 |
| **UMA (FMCA)** | Convergence services over WiFi-GAN | Aug. 2005 |
| **WMM (including WMM Power Save)** | | Ver 1.1 |

*Table 7.2: Applicable WiFi standards*

## 7.3 Regulatory

| Country | Approval authority | Regulatory | Frequency band |
|---|---|---|---|
| **USA** | FCC | FCC ID XO2HDG104 | 2.4 GHz -2.4835 GHz |
| **Canada** | IC | RSS IC: 8713A-SPB105 | 2.4 GHz -2.4835 GHz |
| **Europe** | National | ETSI | 2.4 GHz -2.4835 GHz |
| | | | |

*Table 7.3: Regulatory standards*

### 7.3.1 FCC (United States of America)

This equipment complies with Part 15 of the FCC rules and regulations.
To fulfill FCC Certification requirements, an OEM manufacturer must comply with the following regulations:
1. The modular transmitter must be labeled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following:

**Example of label required for OEM product containing SPB105 module**

| **Contains FCC ID: XO2HDG104** |
| --- |
| The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (i) this device may not cause harmful interference and (ii) this device must accept any interference received, including interference that may cause undesired operation. |

Any similar wording that expresses the same meaning may be used.

2. To be used with the SPB105 module, the external antennas have been tested and approved which are specified in here below. The SPB105 Module may be integrated with custom design antennas which OEM installer must authorize following the FCC 15.21 requirements.

**WARNING:** The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment.

**IMPORTANT:** This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19).

The internal / external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance. This device is approved as a mobile device with respect to RF exposure compliance, and may only be marketed to OEM installers. Use in portable exposure conditions (FCC 2.1093) requires separate equipment authorization.

**IMPORTANT:** Modifications not expressly approved by this company could void the user's uthority to operate this equipment (FCC section 15.21).

**IMPORTANT:** This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to

cause harmful interference in which case the user will be required to correct the interference at his own expense (FCC section 15.105).

### 7.3.2 IC (Canada)

Equipment is subject to certification under the applicable RSSs, shall be permanently labeled on each item, or as an inseparable combination. The label must contain the following information for full compliance:

| | |
|---|---|
| **Certification Number:** | **IC: 8713A-HDG104** |
| **Manufacturer's Name, Trade Name or Brand Name** | **H&D Wireless AB** |
| **Model Name:** | **HDG104** |

**IMPORTANT:** This equipment for which a certificate has been issued is not considered certified if it is not properly labeled. The information on the Canadian label can be combined with the manufacturer's other labeling requirements

**IMPORTANT:** Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

**IMPORTANT:** To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

**IMPORTANT:** The installer of this radio equipment must ensure that the antenna is located or pointed such that it does not emit RF field in excess of Health Canada limits for the general population. Consult Safety Code 6, obtainable from Health Canada's website www.hc-sc.gc.ca/rpb.

### 7.3.3 ETSI (Europe)

The SPB105 module has been certified for use in European union countries according to ETSI EN 300 328 (Electromagnetic compatibility and Radio spectrum matters for equipment operating in the 2,4 GHz ISM band using spread spectrum modulation techniques). This standard is harmonized within the European Union and covering essential requirements under article 3.2 of the R&TTE-directive.

If the SPB105 module are incorporated into a product, the manufacturer must ensure compliance of the final end-user product to the European harmonized EMC and low voltage/safety standards. A declaration of conformity must be issued for the product including compliance references to these standards. Underlying the declaration of conformity a technical construction file (TCF), including all relevant test reports and technical documentation, must be issued and kept on file as described in Annex II of the R&TTE-directive.

Furthermore, the manufacturer must maintain a copy of the SPB105 module documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a complete re-test must be made in order to comply with all relevant standards as basis for CE-marking. A submission to notified body must be used only if deviations from standards have been found or if non-harmonized standards have been used.

# 8 SALES OFFICES

## Global Sales Office Sweden

**H&D Wireless AB**
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Norgegatan 1
164 32 Kista
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Home page: www.hd-wireless.se

## Local sales offices and representatives see www.hd-wireless.se