

**Revision History****AS7C351232-10BIN 90ball TFBGA PACKAGE**

Revision	Details	Date
Rev 1.0	Initial Issue	Jan. 2017

### FEATURES

- Fast access time : 10ns
- **Low power consumption:**  
 Operating current : 125mA (TYP.)  
 Standby current : 4mA (TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : B0# (DQ0 ~ DQ7)  
                           B1# (DQ8 ~ DQ15)  
                           B2# (DQ16~DQ23)  
                           B3# (DQ24~DQ31)
- Data retention voltage : 1.5V (MIN.)
- **ROHS Compliant/Pb & Halogen free**
- Package : 90-ball 8mm x 13mm TFBGA

### GENERAL DESCRIPTION

The AS7C351232-10BIN is a 16M-bit high speed CMOS static random access memory organized as 512K words by 32 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C351232-10BIN operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

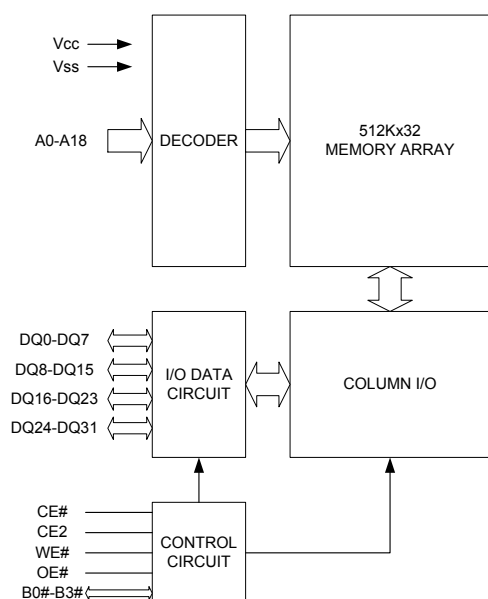
### PRODUCT FAMILY

Product Family	Operating Temperature	V <sub>CC</sub> Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> , TYP.)	Operating(I <sub>CC</sub> , TYP.)
AS7C351232-10BIN	-40 ~ 85°C	2.7 ~ 3.6V	10ns	4mA	125mA

### ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(°C)	Packing Type	Alliance Part Number
90-ball (8mm x 13mm) TFBGA	10	-40°C~85°C	Tray	AS7C351232-10BIN
			Tape Reel	AS7C351232-10BINTR

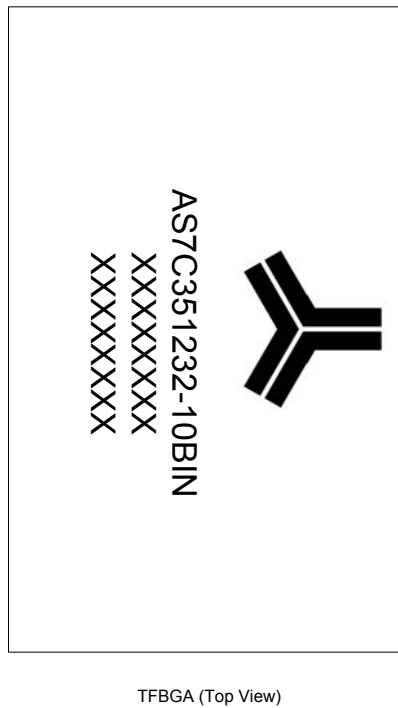
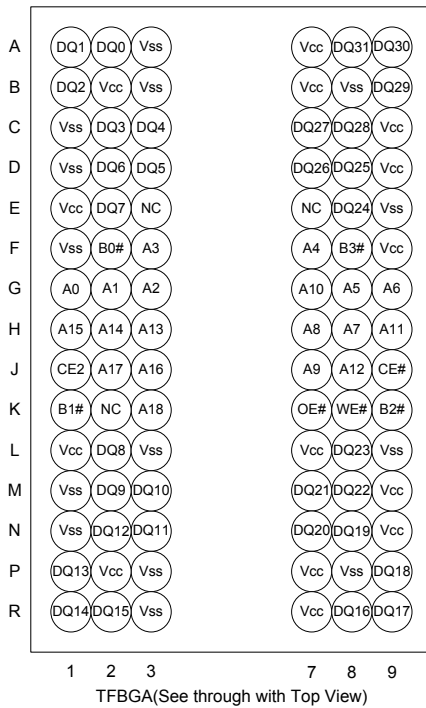
### FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ31	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
B0# - B3#	Byte Control
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground
NC	No Connection

## PIN CONFIGURATION



### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to V <sub>SS</sub>	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	-40 to 85(I grade)	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

### TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	B0#	B1#	B0#	B1#	I/O OPERATION				SUPPLY CURRENT
									DQ0-7	DQ8-15	DQ16-23	DQ24-31	
Standby	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	I <sub>SB1</sub>
	X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	
Output Disable	L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	I <sub>CC</sub>
	L	H	X	X	H	H	H	H	High-Z	High-Z	High-Z	High-Z	
Read	L	H	L	H	L	H	H	H	D <sub>OUT</sub>	High-Z	High-Z	High-Z	I <sub>CC</sub>
	L	H	L	H	H	L	H	H	High-Z	D <sub>OUT</sub>	High-Z	High-Z	
	L	H	L	H	H	H	L	H	High-Z	High-Z	D <sub>OUT</sub>	High-Z	
	L	H	L	H	H	H	H	L	High-Z	High-Z	High-Z	D <sub>OUT</sub>	
	L	H	L	H	L	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	H	X	L	L	H	H	H	D <sub>IN</sub>	High-Z	High-Z	High-Z	I <sub>CC</sub>
	L	H	X	L	H	L	H	H	High-Z	D <sub>IN</sub>	High-Z	High-Z	
	L	H	X	L	H	H	L	H	High-Z	High-Z	D <sub>IN</sub>	High-Z	
	L	H	X	L	H	H	H	L	High-Z	High-Z	High-Z	D <sub>IN</sub>	
	L	H	X	L	L	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	TEST CONDITION	MIN.	TYP. <sup>*4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>		2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>		- 0.3	-	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	- 1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	- 1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	2.4	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V, other pins at 0.2V or V <sub>CC</sub> -0.2V, I <sub>I/O</sub> = 0mA; f=max.	-10	-	125	180	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V; other pins at 0.2V or V <sub>CC</sub> -0.2V.	-	4	40	mA	

Notes:

1. V<sub>IH</sub>(MAX.) = V<sub>CC</sub> + 2.0V for pulse width less than 6ns.
2. V<sub>IL</sub>(MIN.) = V<sub>SS</sub> - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

### CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

Speed	10 ns
Input Pulse Levels	0.2V to V <sub>CC</sub> -0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	V <sub>CC</sub> /2
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -4mA/8mA

### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

PARAMETER	SYM.	AS7C351232-10BIN		UNIT
		MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	10	-	ns
Address Access Time	t <sub>AA</sub>	-	10	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	10	ns
Output Enable Access Time	t <sub>OE</sub>	-	4.5	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	2	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	4	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	4	ns
Output Hold from Address Change	t <sub>OH</sub>	2	-	ns
Byte Control Access Time	t <sub>BA</sub>	-	4.5	ns
Byte Control to High-Z Output	t <sub>BHZ</sub> *	-	4	ns
Byte Control to Low-Z Output	t <sub>BLZ</sub> *	0	-	ns

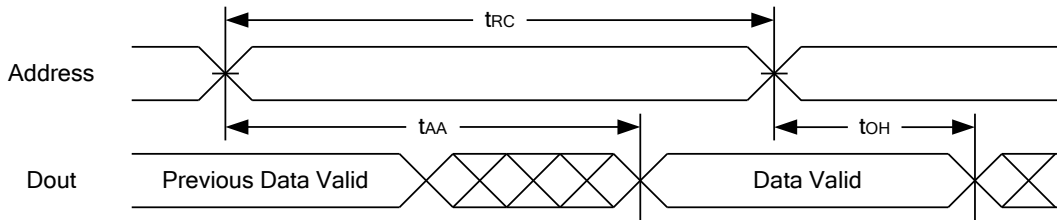
#### (2) WRITE CYCLE

PARAMETER	SYM.	AS7C351232-10BIN		UNIT
		MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	10	-	ns
Address Valid to End of Write	t <sub>AW</sub>	8	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	8	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	ns
Write Pulse Width	t <sub>WP</sub>	8	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	6	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	2	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	4	ns
Byte Control Valid to End of Write	t <sub>BW</sub>	8	-	ns

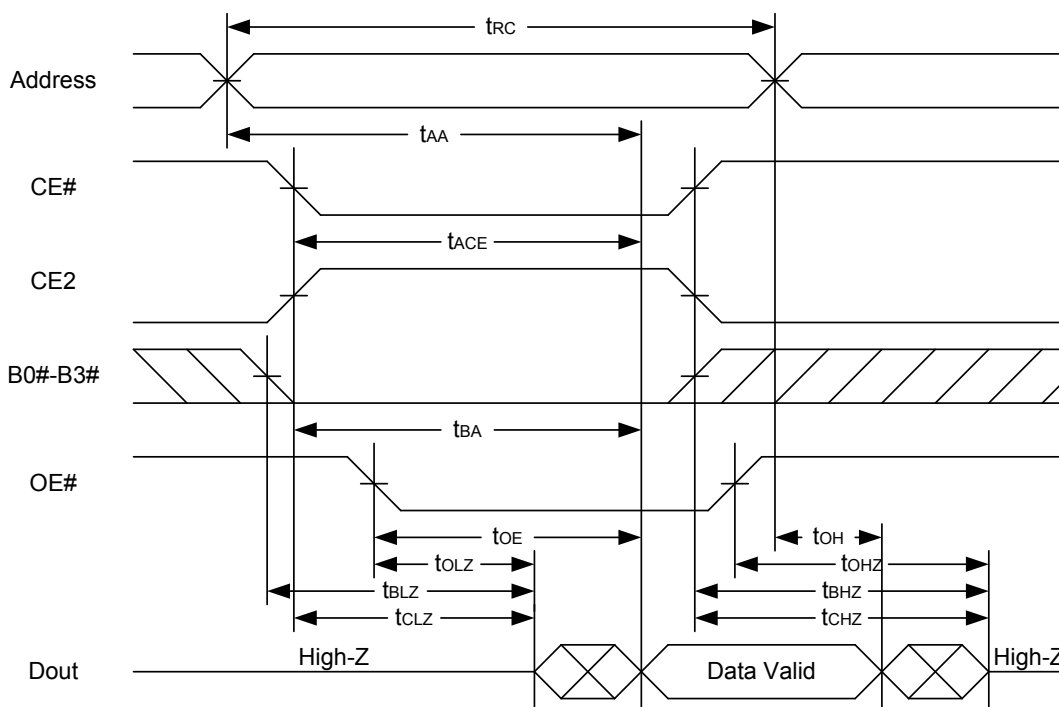
\*These parameters are guaranteed by device characterization, but not production tested.

### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



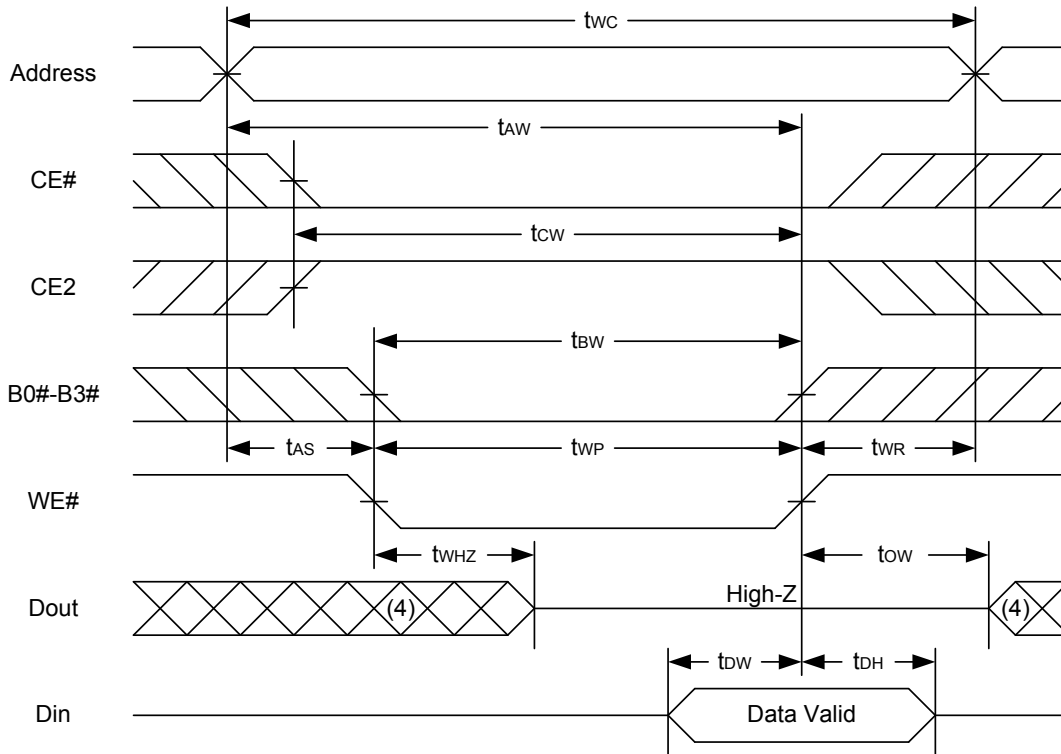
#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



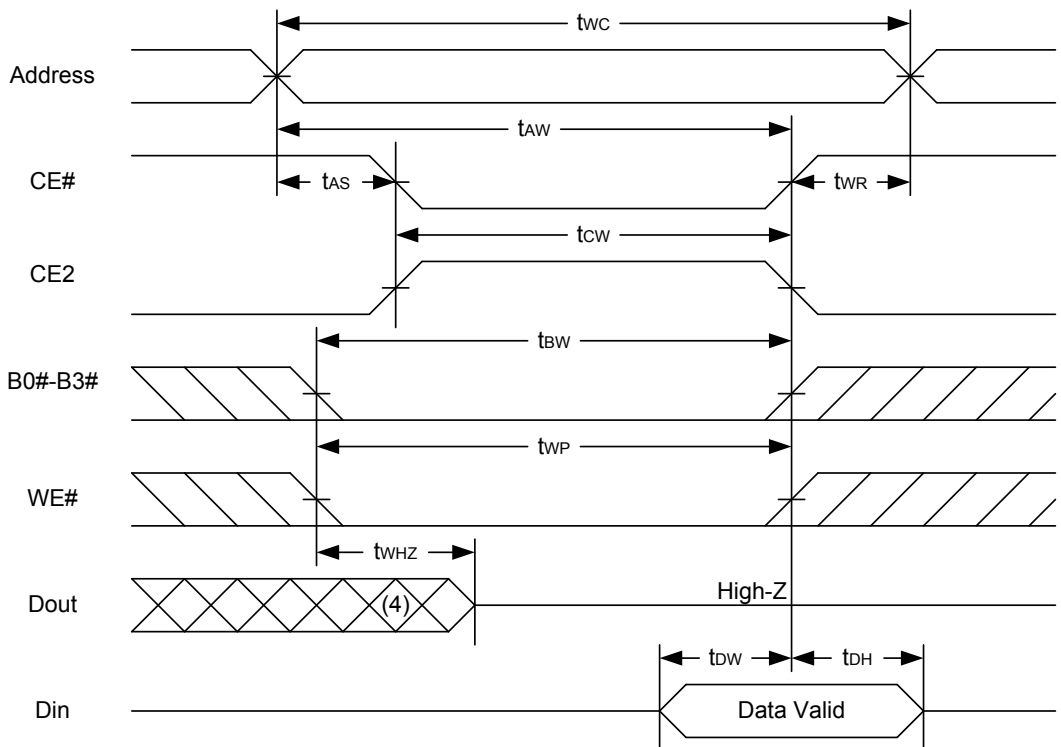
**Notes :**

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

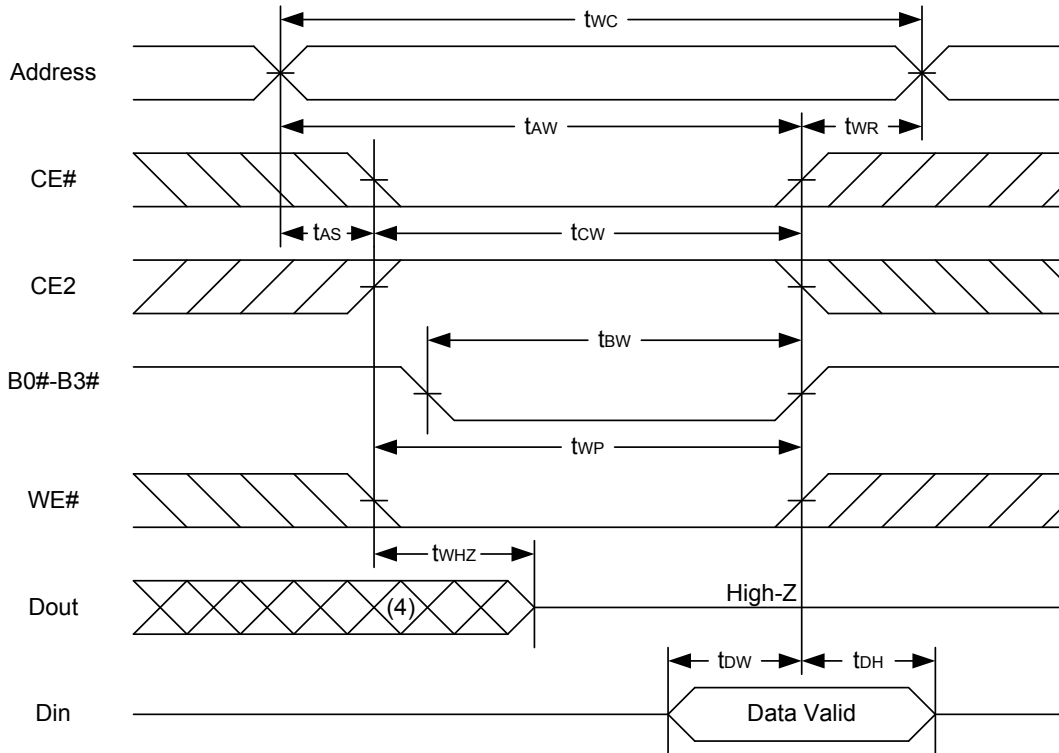


### WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)





### WRITE CYCLE 3 (B0# ~ B3# Controlled) (1,4,5)



**Notes :**

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, and B0#, B1#, B2# or B3# = low.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, B0# ~ B3# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.

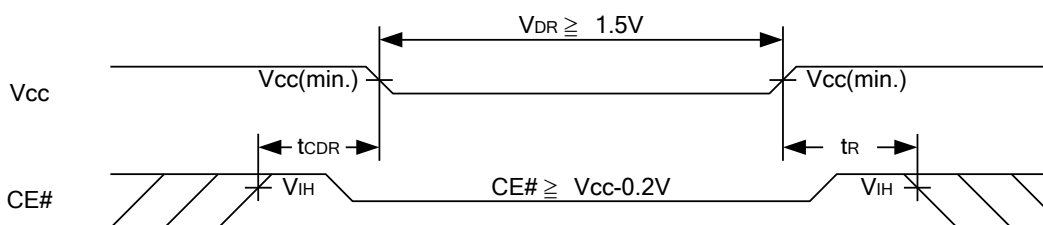
### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# ≥ V <sub>CC</sub> - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	-	4	40	mA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns

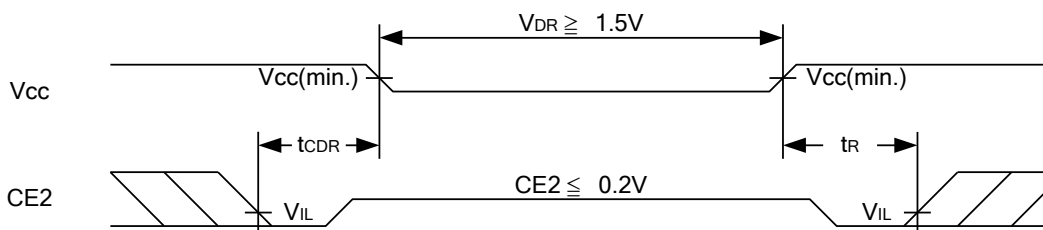
t<sub>RC</sub>\* = Read Cycle Time

### DATA RETENTION WAVEFORM

**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**

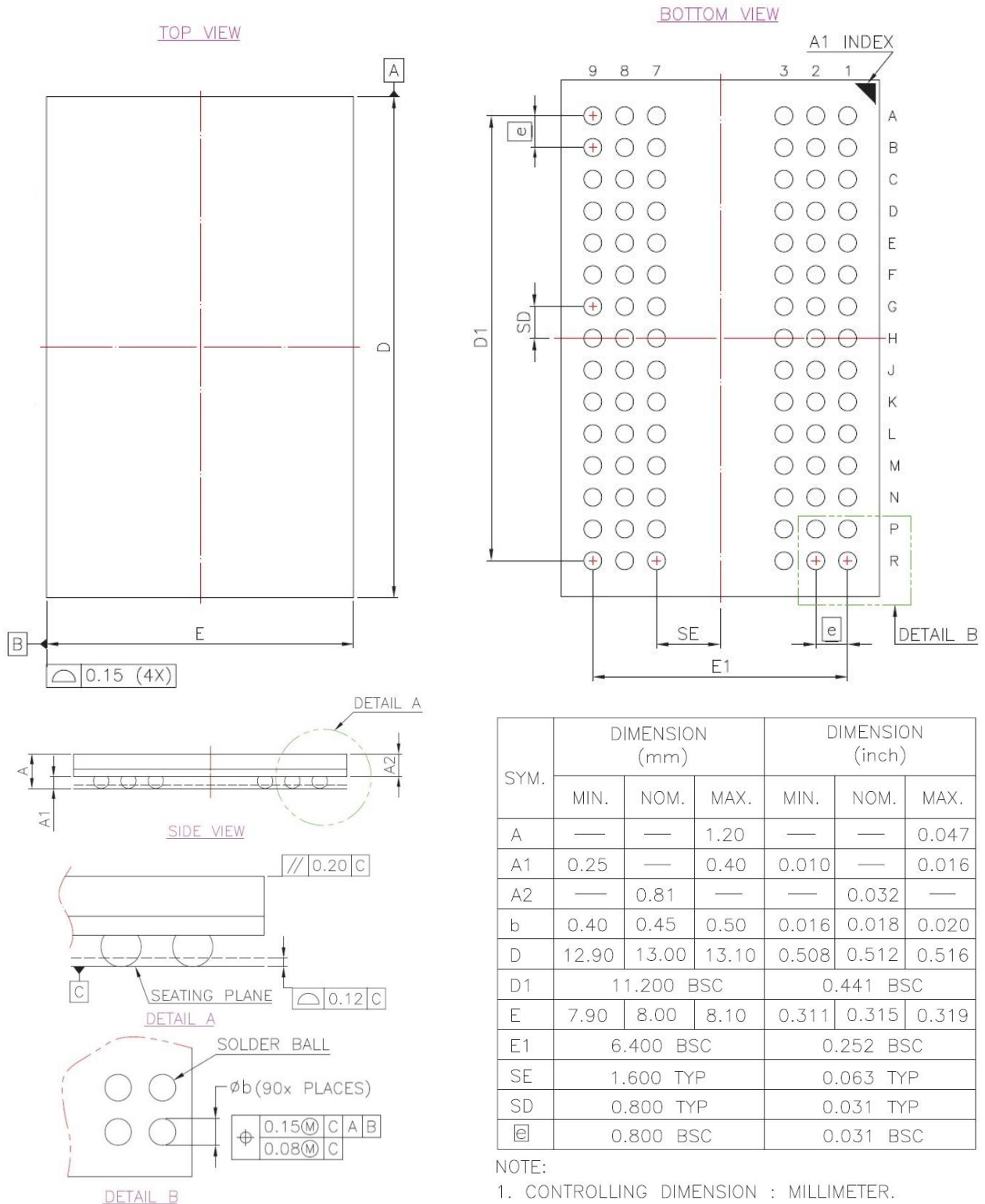


**Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)**



### PACKAGE OUTLINE DIMENSION

#### 90-ball 8mm x 13mm TFBGA Package Outline Dimension



### PART NUMBERING SYSTEM

AS7C	351232	10	B	I	N
SRAM	3=3.3v 51232=512K x 32	10=10 ns	B = TFBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free



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