

SSTU32864

1.8 V configurable registered buffer for DDR2 RDIMM applications

Rev. 02 — 22 October 2004

Product data sheet

1. General description

The SSTU32864 is a 25-bit 1:1 or 14-bit 1:2 configurable registered buffer designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32864 operates from a differential clock (CK and \overline{CK}). Data are registered at the crossing of CK going HIGH, and \overline{CK} going LOW.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1:1 (when LOW) to 14-bit 1:2 (when HIGH).

The device supports low-power standby operation. When the reset input (\overline{RESET}) is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when \overline{RESET} is LOW all registers are reset, and all outputs are forced LOW. The LVCMOS \overline{RESET} and Cn inputs must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, \overline{RESET} must be held in the LOW state during power-up.

In the DDR2 RDIMM application, \overline{RESET} is specified to be completely asynchronous with respect to CK and \overline{CK} . Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of \overline{RESET} until the input receivers are fully enabled, the design of the SSTU32864 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

The device monitors both \overline{DCS} and \overline{CSR} inputs and will gate the Qn outputs from changing states when both \overline{DCS} and \overline{CSR} inputs are HIGH. If either \overline{DCS} or \overline{CSR} input is LOW, the Qn outputs will function normally. The \overline{RESET} input has priority over the \overline{DCS} and \overline{CSR} control and will force the outputs LOW. If the \overline{DCS} -control functionality is not desired, then the \overline{CSR} input can be hardwired to ground, in which case the setup time requirement for \overline{DCS} would be the same as for the other Dn data inputs.

The SSTU32864 is available in a 96-ball, low profile fine-pitch ball grid array (LFBGA96) package.

The Philips logo, consisting of the word "PHILIPS" in a bold, blue, sans-serif font.

2. Features

- Configurable register supporting DDR2 Registered DIMM applications
- Configurable to 25-bit 1:1 mode or 14-bit 1:2 mode
- Controlled output impedance drivers enable optimal signal integrity and speed
- Exceeds JESD82-7 speed performance (1.8 ns max. single-bit switching propagation delay; 2.0 ns max. mass-switching)
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports SSTL_18 data inputs
- Differential clock (CK and $\overline{\text{CK}}$) inputs
- Supports LVCMOS switching levels on the control and $\overline{\text{RESET}}$ inputs
- Single 1.8 V supply operation
- Available in 96-ball, 13.5 × 5.5 mm, 0.8 mm ball pitch LFBGA package

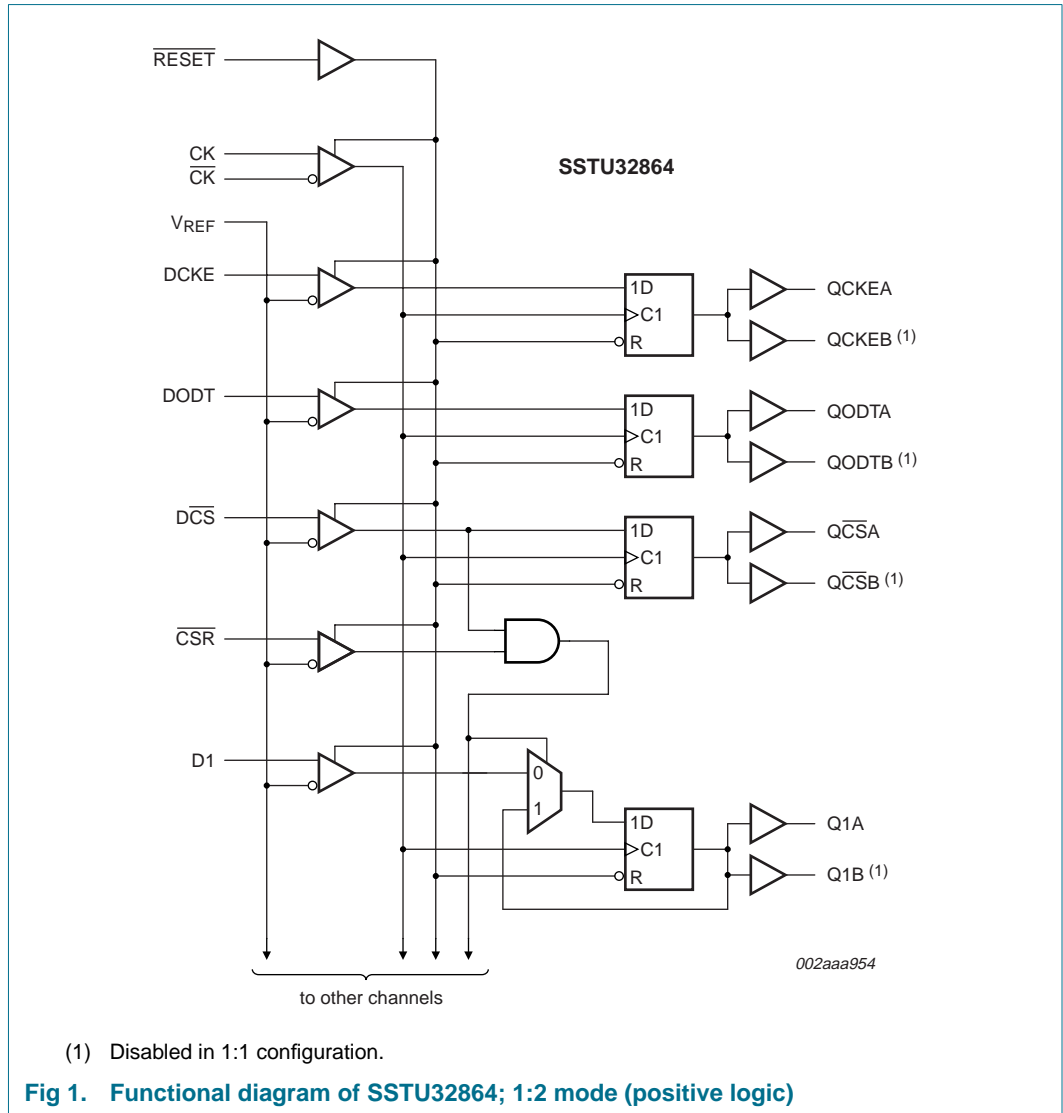
3. Ordering information

Table 1: Ordering information

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$.

| Type number | Solder process | Package | | |
|---------------|---------------------------------------|---------|---|----------|
| | | Name | Description | Version |
| SSTU32864EC/G | Pb-free (SnAgCu solder ball compound) | LFBGA96 | plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm | SOT536-1 |
| SSTU32864EC | SnPb solder ball compound | LFBGA96 | plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm | SOT536-1 |

4. Functional diagram



5. Pinning information

5.1 Pinning

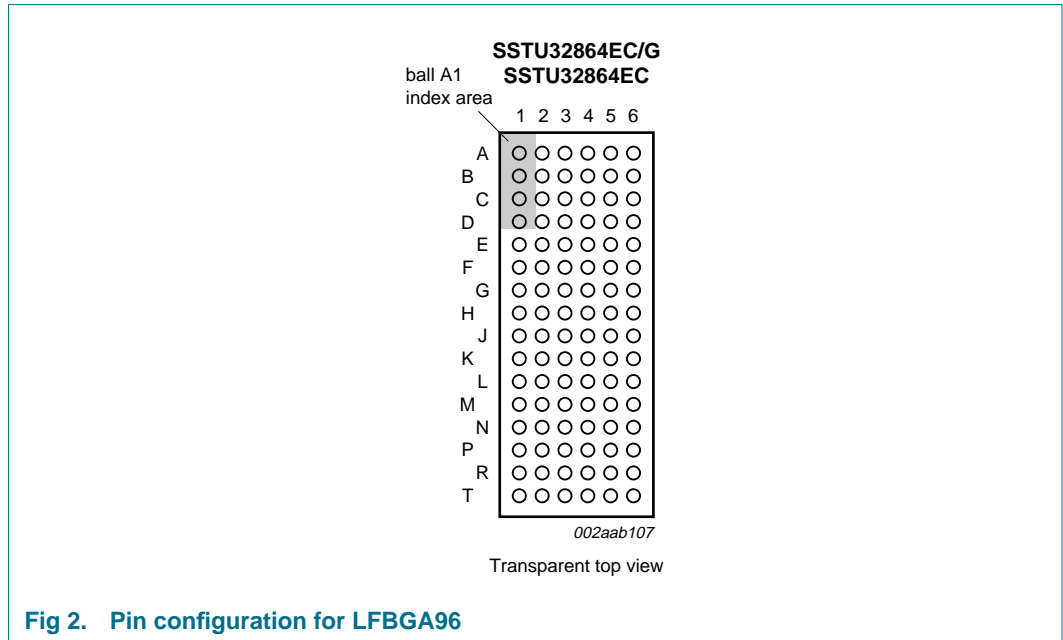


Fig 2. Pin configuration for LFBGA96

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------------|---------------------------|------------------|-----------------|-------------------------|--------|
| A | DCKE | n.c. | V _{REF} | V _{DD} | QCKE | d.n.u. |
| B | D2 | D15 | GND | GND | Q2 | Q15 |
| C | D3 | D16 | V _{DD} | V _{DD} | Q3 | Q16 |
| D | DODT | n.c. | GND | GND | QODT | d.n.u. |
| E | D5 | D17 | V _{DD} | V _{DD} | Q5 | Q17 |
| F | D6 | D18 | GND | GND | Q6 | Q18 |
| G | n.c. | $\overline{\text{RESET}}$ | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | $\overline{\text{DCS}}$ | GND | GND | $\overline{\text{QCS}}$ | d.n.u. |
| J | $\overline{\text{CK}}$ | $\overline{\text{CSR}}$ | V _{DD} | V _{DD} | ZOH | ZOL |
| K | D8 | D19 | GND | GND | Q8 | Q19 |
| L | D9 | D20 | V _{DD} | V _{DD} | Q9 | Q20 |
| M | D10 | D21 | GND | GND | Q10 | Q21 |
| N | D11 | D22 | V _{DD} | V _{DD} | Q11 | Q22 |
| P | D12 | D23 | GND | GND | Q12 | Q23 |
| R | D13 | D24 | V _{DD} | V _{DD} | Q13 | Q24 |
| T | D14 | D25 | V _{REF} | V _{DD} | Q14 | Q25 |

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Fig 3. Ball mapping; 1:1 register (C0 = 0, C1 = 0); top view

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------------|---------------------------|------------------|-----------------|--------------------------|--------------------------|
| A | DCKE | n.c. | V _{REF} | V _{DD} | QCKEA | QCKEB |
| B | D2 | d.n.u. | GND | GND | Q2A | Q2B |
| C | D3 | d.n.u. | V _{DD} | V _{DD} | Q3A | Q3B |
| D | DODT | n.c. | GND | GND | QODTA | QODTB |
| E | D5 | d.n.u. | V _{DD} | V _{DD} | Q5A | Q5B |
| F | D6 | d.n.u. | GND | GND | Q6A | Q6B |
| G | n.c. | $\overline{\text{RESET}}$ | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | $\overline{\text{DCS}}$ | GND | GND | $\overline{\text{QCSA}}$ | $\overline{\text{QCSB}}$ |
| J | $\overline{\text{CK}}$ | $\overline{\text{CSR}}$ | V _{DD} | V _{DD} | ZOH | ZOL |
| K | D8 | d.n.u. | GND | GND | Q8A | Q8B |
| L | D9 | d.n.u. | V _{DD} | V _{DD} | Q9A | Q9B |
| M | D10 | d.n.u. | GND | GND | Q10A | Q10B |
| N | D11 | d.n.u. | V _{DD} | V _{DD} | Q11A | Q11B |
| P | D12 | d.n.u. | GND | GND | Q12A | Q12B |
| R | D13 | d.n.u. | V _{DD} | V _{DD} | Q13A | Q13B |
| T | D14 | d.n.u. | V _{REF} | V _{DD} | Q14A | Q14B |

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Fig 4. Ball mapping; 1:2 register A (C0 = 0, C1 = 1); top view

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------------|---------------------------|------------------|-----------------|--------------------------|--------------------------|
| A | D1 | n.c. | V _{REF} | V _{DD} | Q1A | Q1B |
| B | D2 | d.n.u. | GND | GND | Q2A | Q2B |
| C | D3 | d.n.u. | V _{DD} | V _{DD} | Q3A | Q3B |
| D | D4 | n.c. | GND | GND | Q4A | Q4B |
| E | D5 | d.n.u. | V _{DD} | V _{DD} | Q5A | Q5B |
| F | D6 | d.n.u. | GND | GND | Q6A | Q6B |
| G | n.c. | $\overline{\text{RESET}}$ | V _{DD} | V _{DD} | C1 | C0 |
| H | CK | $\overline{\text{DCS}}$ | GND | GND | $\overline{\text{QCSA}}$ | $\overline{\text{QCSB}}$ |
| J | $\overline{\text{CK}}$ | $\overline{\text{CSR}}$ | V _{DD} | V _{DD} | ZOH | ZOL |
| K | D8 | d.n.u. | GND | GND | Q8A | Q8B |
| L | D9 | d.n.u. | V _{DD} | V _{DD} | Q9A | Q9B |
| M | D10 | d.n.u. | GND | GND | Q10A | Q10B |
| N | DODT | d.n.u. | V _{DD} | V _{DD} | QODTA | QODTB |
| P | D12 | d.n.u. | GND | GND | Q12A | Q12B |
| R | D13 | d.n.u. | V _{DD} | V _{DD} | Q13A | Q13B |
| T | DCKE | d.n.u. | V _{REF} | V _{DD} | QCKEA | QCKEB |

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Fig 5. Ball mapping; 1:2 register B (C0 = 1, C1 = 1); top view

5.2 Pin description

Table 2: Pin description

| Symbol | Pin | Type | Description |
|---|---|--------------------|---|
| GND | B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4 | ground input | ground |
| V _{DD} | A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4 | 1.8 V nominal | power supply voltage |
| V _{REF} | A3, T3 | 0.9 V nominal | input reference voltage |
| ZOH | J5 | input | reserved for future use |
| ZOL | J6 | input | reserved for future use |
| CK | H1 | differential input | positive master clock input |
| \overline{CK} | J1 | differential input | negative master clock input |
| C0, C1 | G6, G5 | LVC MOS inputs | configuration control inputs |
| \overline{RESET} | G2 | LVC MOS input | Asynchronous reset input. Resets registers and disables V _{REF} data and clock differential-input receivers. |
| \overline{CSR} , \overline{DCS} | J2, H2 | SSTL_18 input | Chip select inputs. Disables data outputs switching when both inputs are HIGH. [2] |
| D1 to D25 | [1] | SSTL_18 input | Data inputs. Clocked in on the crossing of the rising edge of CK and the falling edge of \overline{CK} . |
| DODT | [1] | SSTL_18 input | The outputs of this register will not be suspended by \overline{DCS} and \overline{CSR} control. |
| DCKE | [1] | SSTL_18 input | The outputs of this register will not be suspended by \overline{DCS} and \overline{CSR} control. |
| Q1 to Q25, Q1A to Q14A, Q1B to Q14B | [1] | 1.8 V CMOS | The outputs that are suspended by \overline{DCS} and \overline{CSR} control. [3] |
| \overline{QCS} , $\overline{QC SA}$, QCSB | [1] | 1.8 V CMOS | Data outputs that will not be suspended by \overline{DCS} and \overline{CSR} control. |
| QODT, QODTA, QODTB | [1] | 1.8 V CMOS | Data outputs that will not be suspended by \overline{DCS} and \overline{CSR} control. |
| QCKE, QCKEA, QCKEB | [1] | 1.8 V CMOS | Data outputs that will not be suspended by \overline{DCS} and \overline{CSR} control. |
| n.c. | A2, D2, G1 | - | Not connected. Ball present but no internal connection to the die. |
| d.n.u. | [1] | - | Do-not-use. Ball internally connected to the die which should be left open-circuit. |

[1] Depends on configuration. Refer to [Figure 3](#), [Figure 4](#), and [Figure 5](#) for ball number.

[2] Configurations:

Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.

Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.

Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[3] Configurations:

Data outputs = Q2, Q3, Q5, Q6, Q8 to Q25 when C0 = 0 and C1 = 0.

Data outputs = Q2, Q3, Q5, Q6, Q8 to Q14 when C0 = 0 and C1 = 1.

Data outputs = Q1 to Q6, Q8 to Q10, Q12, Q13 when C0 = 1 and C1 = 1.

6. Functional description

6.1 Function table

Table 3: Function table (each flip-flop)

| Inputs | | | | | | Outputs ^[1] | | |
|--------|------------------|------------------|------------------|------------------|----------------------|------------------------|----------------|----------------|
| RESET | DCS | CSR | CK | CK | Dn, DODT, DCKE | Qn | QCS | QODT, QCKE |
| H | L | L | ↑ | ↓ | L | L | L | L |
| H | L | L | ↑ | ↓ | H | H | L | H |
| H | L | L | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | L | H | ↑ | ↓ | L | L | L | L |
| H | L | H | ↑ | ↓ | H | H | L | H |
| H | L | H | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | H | L | ↑ | ↓ | L | L | H | L |
| H | H | L | ↑ | ↓ | H | H | H | H |
| H | H | L | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| H | H | H | ↑ | ↓ | L | Q ₀ | H | L |
| H | H | H | ↑ | ↓ | H | Q ₀ | H | H |
| H | H | H | L or H | L or H | X | Q ₀ | Q ₀ | Q ₀ |
| L | X or floating | X or floating | X or floating | X or floating | X or floating | L | L | L |

[1] Q₀ is the previous state of the associated output.

H — HIGH voltage level

L — LOW voltage level

↓ — HIGH-to-LOW transition

↑ — LOW-to-HIGH transition

X — Don't care

7. Limiting values

Table 4: Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---|--------------------------------------|----------|--------------------|------|
| V_{DD} | supply voltage | | -0.5 | +2.5 | V |
| V_I | receiver input voltage | | -0.5 [2] | +2.5 [3] | V |
| V_O | driver output voltage | | -0.5 [2] | $V_{DD} + 0.5$ [3] | V |
| I_{IK} | input clamp current | $V_I < 0\text{ V}$ or $V_I > V_{DD}$ | - | ± 50 | mA |
| I_{OK} | output clamp current | $V_O < 0\text{ V}$ or $V_O > V_{DD}$ | - | ± 50 | mA |
| I_O | continuous output current | $0\text{ V} < V_O < V_{DD}$ | - | ± 50 | mA |
| I_{CCC} | continuous current through each V_{DD} or GND pin | | - | ± 100 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |

- [1] Stresses beyond those listed under 'absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 'recommended operating conditions' is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [2] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- [3] This value is limited to 2.5 V maximum.

8. Recommended operating conditions

Table 5: Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---|---------------------------------------|----------------------------|----------------------|----------------------------|------|
| V_{DD} | supply voltage | | 1.7 | - | 1.9 | V |
| V_{REF} | reference voltage | | $0.49 \times V_{DD}$ | $0.50 \times V_{DD}$ | $0.51 \times V_{DD}$ | V |
| V_{TT} | termination voltage | | $V_{REF} - 40 \text{ mV}$ | V_{REF} | $V_{REF} + 40 \text{ mV}$ | V |
| V_I | input voltage | | 0 | - | V_{DD} | V |
| $V_{IH(AC)}$ | AC HIGH-level input voltage | data inputs (Dn), \overline{CSR} | $V_{REF} + 250 \text{ mV}$ | - | - | V |
| $V_{IL(AC)}$ | AC LOW-level input voltage | data inputs (Dn), \overline{CSR} | - | - | $V_{REF} - 250 \text{ mV}$ | V |
| $V_{IH(DC)}$ | DC HIGH-level input voltage | data inputs (Dn), \overline{CSR} | $V_{REF} + 125 \text{ mV}$ | - | - | V |
| $V_{IL(DC)}$ | DC LOW-level input voltage | data inputs (Dn), \overline{CSR} | - | - | $V_{REF} - 125 \text{ mV}$ | V |
| V_{IH} | HIGH-level input voltage | \overline{RESET} , Cn | [1] $0.65 \times V_{DD}$ | - | V_{DD} | V |
| V_{IL} | LOW-level input voltage | \overline{RESET} , Cn | [1] - | - | $0.35 \times V_{DD}$ | V |
| V_{ICR} | common mode input voltage range | CK, \overline{CK} | [2] 0.675 | - | 1.125 | V |
| V_{ID} | differential input voltage | CK, \overline{CK} | [2] 600 | - | - | mV |
| I_{OH} | HIGH-level output current | | - | - | -8 | mA |
| I_{OL} | LOW-level output current | | - | - | 8 | mA |
| T_{amb} | operating ambient temperature in free air | | 0 | - | +70 | °C |

[1] The \overline{RESET} and Cn inputs of the device must be held at valid logic levels (not floating) to ensure proper device operation.

[2] The differential inputs must not be floating, unless \overline{RESET} is LOW.

9. Characteristics

Table 6: Characteristics

Recommended operating conditions, unless otherwise specified. Voltages are referenced to GND (ground = 0 V).
 $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--|--|-----|-----|-----|---------------|
| V_{OH} | HIGH-level output voltage | $I_{OH} = -6\text{ mA}$; $V_{DD} = 1.7\text{ V}$ | 1.2 | - | - | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 6\text{ mA}$; $V_{DD} = 1.7\text{ V}$ | - | - | 0.5 | V |
| I_I | input current | all inputs; $V_I = V_{DD}$ or GND; $V_{DD} = 1.9\text{ V}$ | -5 | - | +5 | μA |
| I_{DD} | static standby current | $\overline{\text{RESET}} = \text{GND}$; $I_O = 0\text{ mA}$; $V_{DD} = 1.9\text{ V}$ | - | - | 100 | μA |
| | static operating current | $\overline{\text{RESET}} = V_{DD}$; $I_O = 0\text{ mA}$; $V_{DD} = 1.9\text{ V}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ | - | - | 40 | mA |
| I_{DDD} | dynamic operating current per MHz, clock only | $\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle. $I_O = 0\text{ mA}$; $V_{DD} = 1.9\text{ V}$ | - | 16 | - | μA |
| | dynamic operating current per MHz, per each data input, 1:1 mode | $\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. $I_O = 0\text{ mA}$; $V_{DD} = 1.9\text{ V}$ | - | 11 | - | μA |
| | dynamic operating current per MHz, per each data input, 1:2 mode | $\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. $I_O = 0\text{ mA}$; $V_{DD} = 1.9\text{ V}$ | - | 19 | - | μA |
| C_i | input capacitance, data inputs, $\overline{\text{CSR}}$ | $V_I = V_{REF} \pm 250\text{ mV}$; $V_{DD} = 1.8\text{ V}$ | 2.5 | - | 3.5 | pF |
| | input capacitance, CK and $\overline{\text{CK}}$ | $V_{ICR} = 0.9\text{ V}$; $V_{ID} = 600\text{ mV}$; $V_{DD} = 1.8\text{ V}$ | 2 | - | 3 | pF |
| | input capacitance, $\overline{\text{RESET}}$ | $V_I = V_{DD}$ or GND; $V_{DD} = 1.8\text{ V}$ | 2 | - | 4 | pF |

Table 7: Timing requirements

Recommended operating conditions; $V_{DD} = 1.8 V \pm 0.1 V$; $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$; unless otherwise specified. See [Figure 6](#) through [Figure 11](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|---|---|--------|-----|-----|------|
| f_{clock} | clock frequency | | - | - | 450 | MHz |
| t_W | pulse duration, CK, \overline{CK} HIGH or LOW | | 1 | - | - | ns |
| t_{ACT} | differential inputs active time | | [1][2] | - | 10 | ns |
| t_{INACT} | differential inputs inactive time | | [1][3] | - | 15 | ns |
| t_{su} | set-up time | \overline{DCS} before CK \uparrow , \overline{CK} \downarrow , \overline{CSR} HIGH | 0.7 | - | - | ns |
| | | \overline{DCS} before CK \uparrow , \overline{CK} \downarrow , \overline{CSR} LOW | 0.5 | - | - | ns |
| | | \overline{CSR} , ODT, CKE, and data before CK \uparrow , CK \downarrow | 0.5 | - | - | ns |
| t_h | hold time | \overline{DCS} , \overline{CSR} , ODT, CKE, and data after CK \uparrow , \overline{CK} \downarrow | 0.5 | - | - | ns |

- [1] This parameter is not necessarily production tested.
- [2] Data inputs must be active below a minimum time of $t_{ACT(max)}$ after \overline{RESET} is taken HIGH.
- [3] Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT(max)}$ after \overline{RESET} is taken LOW.

Table 8: Switching characteristics

Recommended operating conditions; $V_{DD} = 1.8 V \pm 0.1 V$; $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$; Class I, $V_{REF} = V_{TT} = V_{DD} \times 0.5$ and $C_L = 10 pF$; unless otherwise specified. See [Figure 6](#) through [Figure 11](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-------------|---|----------------------------------|--------|------|-----|------|----|
| f_{MAX} | maximum input clock frequency | | 450 | - | - | MHz | |
| t_{PDM} | propagation delay | CK and \overline{CK} to output | [1] | 1.41 | - | 1.8 | ns |
| t_{PDMSS} | propagation delay, simultaneous switching | CK and \overline{CK} to output | [1][2] | - | - | 2.0 | ns |
| t_{PHL} | propagation delay | \overline{RESET} to output | - | - | 3 | ns | |

- [1] Includes 350 ps of test-load transmission line delay.
- [2] This parameter is not necessarily production tested.

Table 9: Output edge rates

Recommended operating conditions, unless otherwise specified. $V_{DD} = 1.8 V \pm 0.1 V$

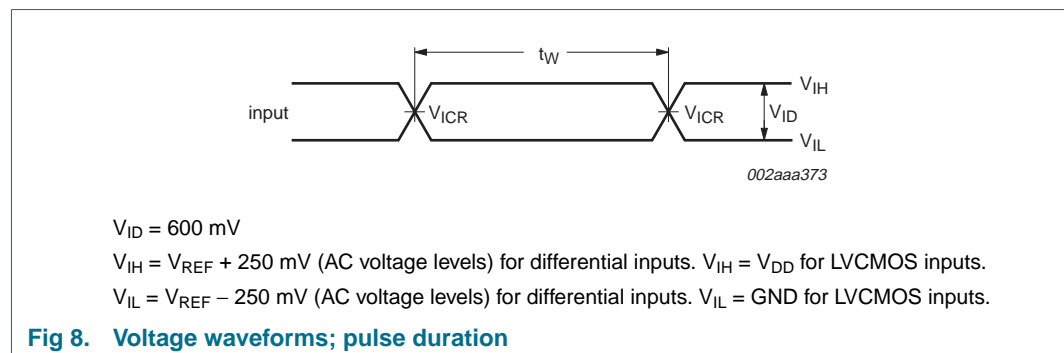
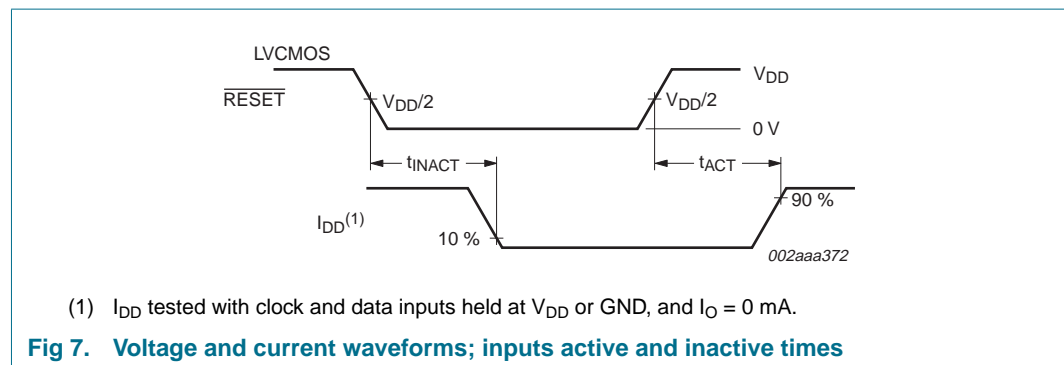
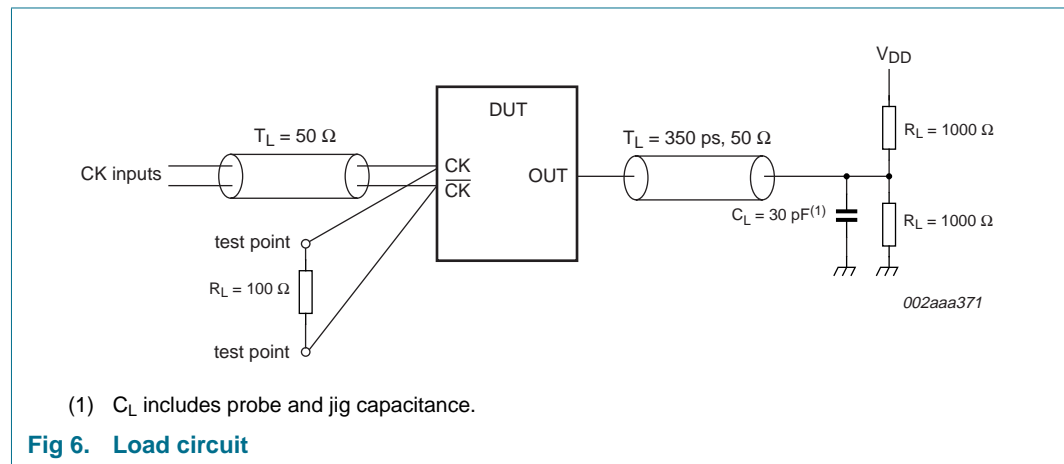
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|------------|-----|-----|-----|------|
| dV/dt_r | rising edge slew rate | | 1 | - | 4 | V/ns |
| dV/dt_f | falling edge slew rate | | 1 | - | 4 | V/ns |
| dV/dt_{Δ} | absolute difference between dV/dt_r and dV/dt_f | | - | - | 1 | V/ns |

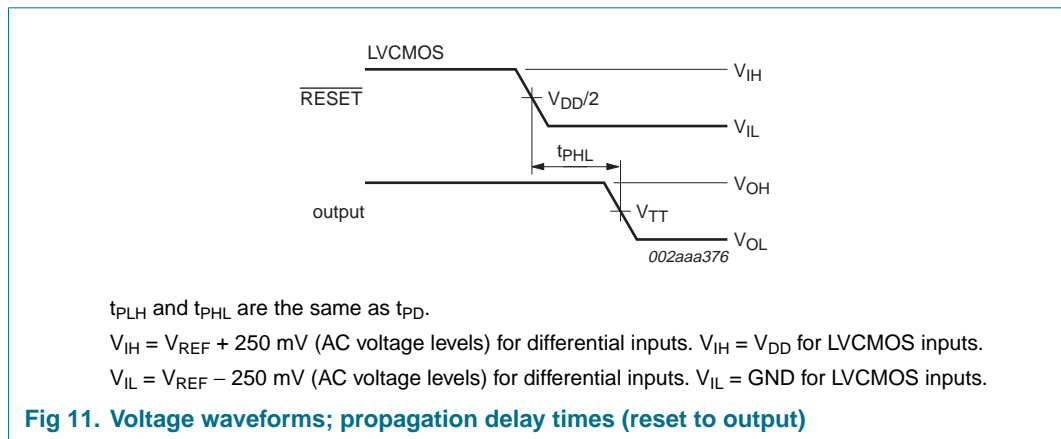
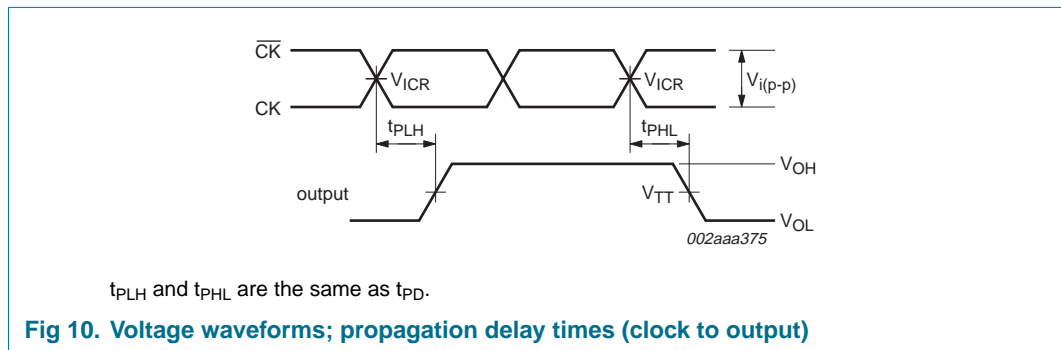
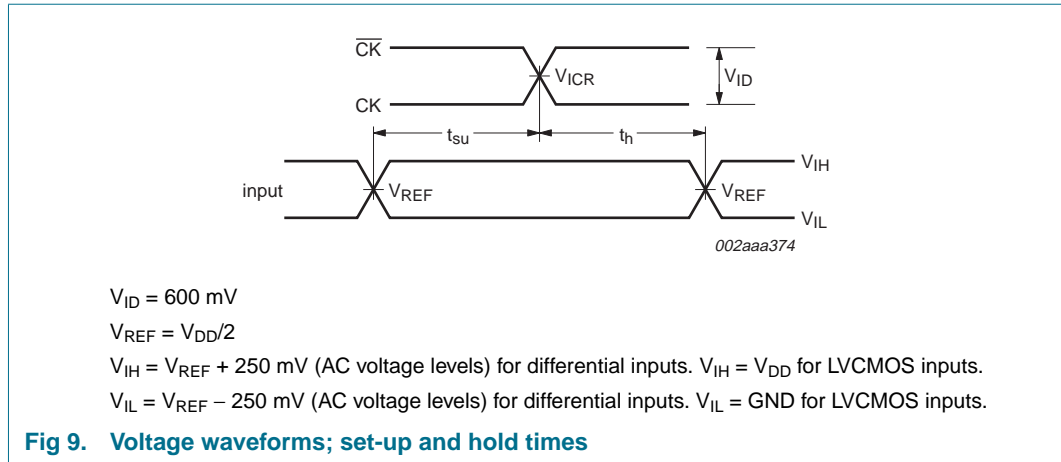
10. Test information

10.1 Test circuit

All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz; $Z_0 = 50 \Omega$; input slew rate = 1 V/ns \pm 20 %, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

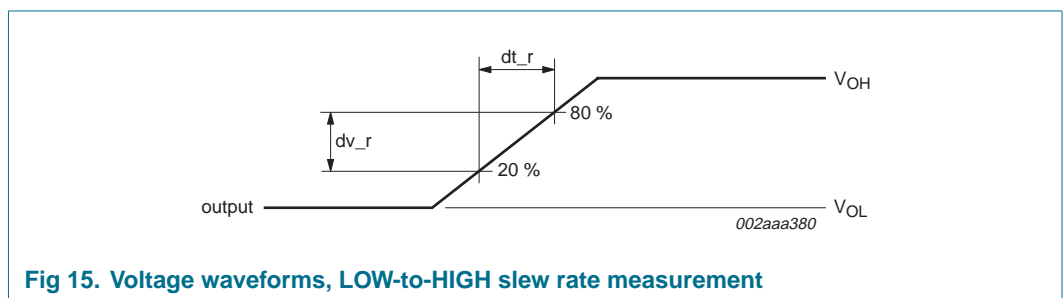
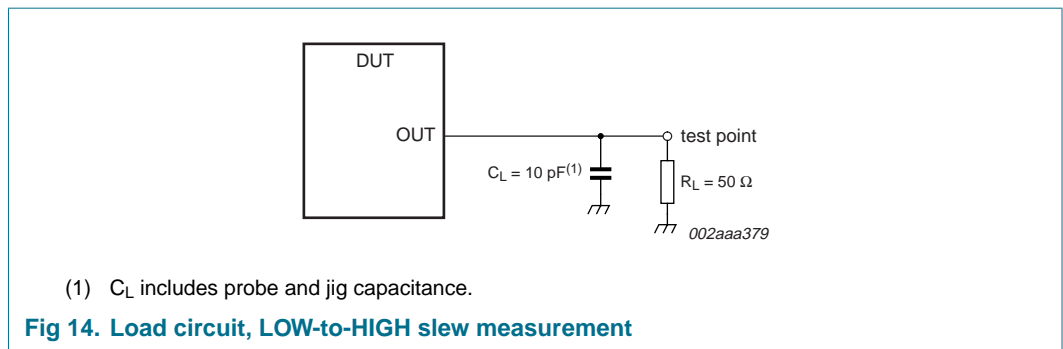
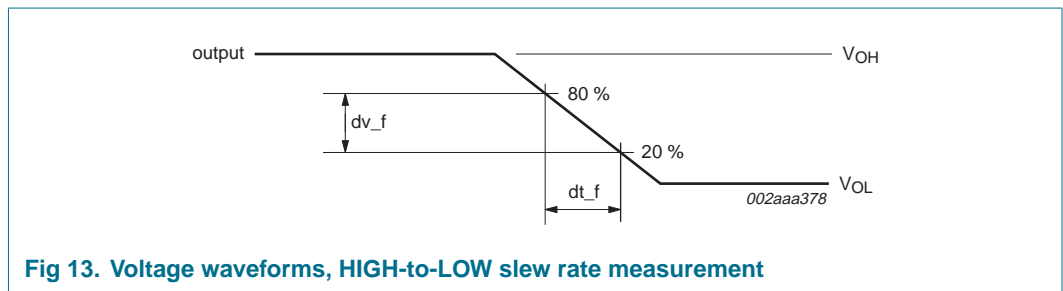
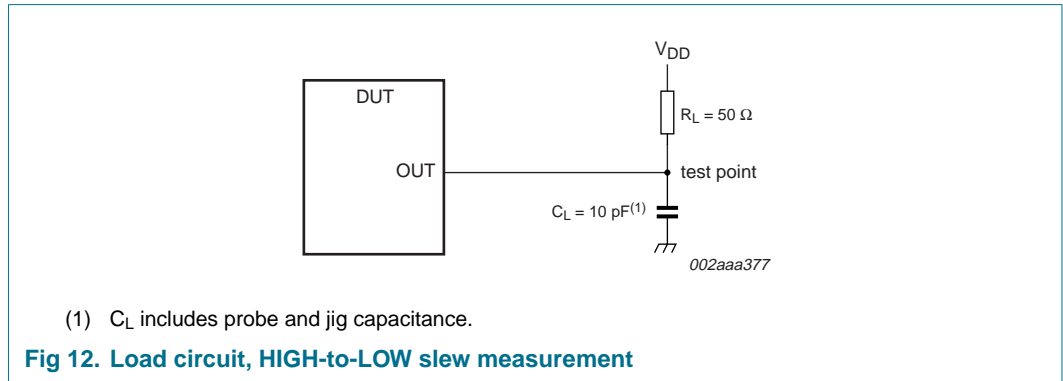




10.2 Output slew rate measurement

$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$.

All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$; $Z_0 = 50\ \Omega$; input slew rate = $1\text{ V/ns} \pm 20\%$, unless otherwise specified.



11. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

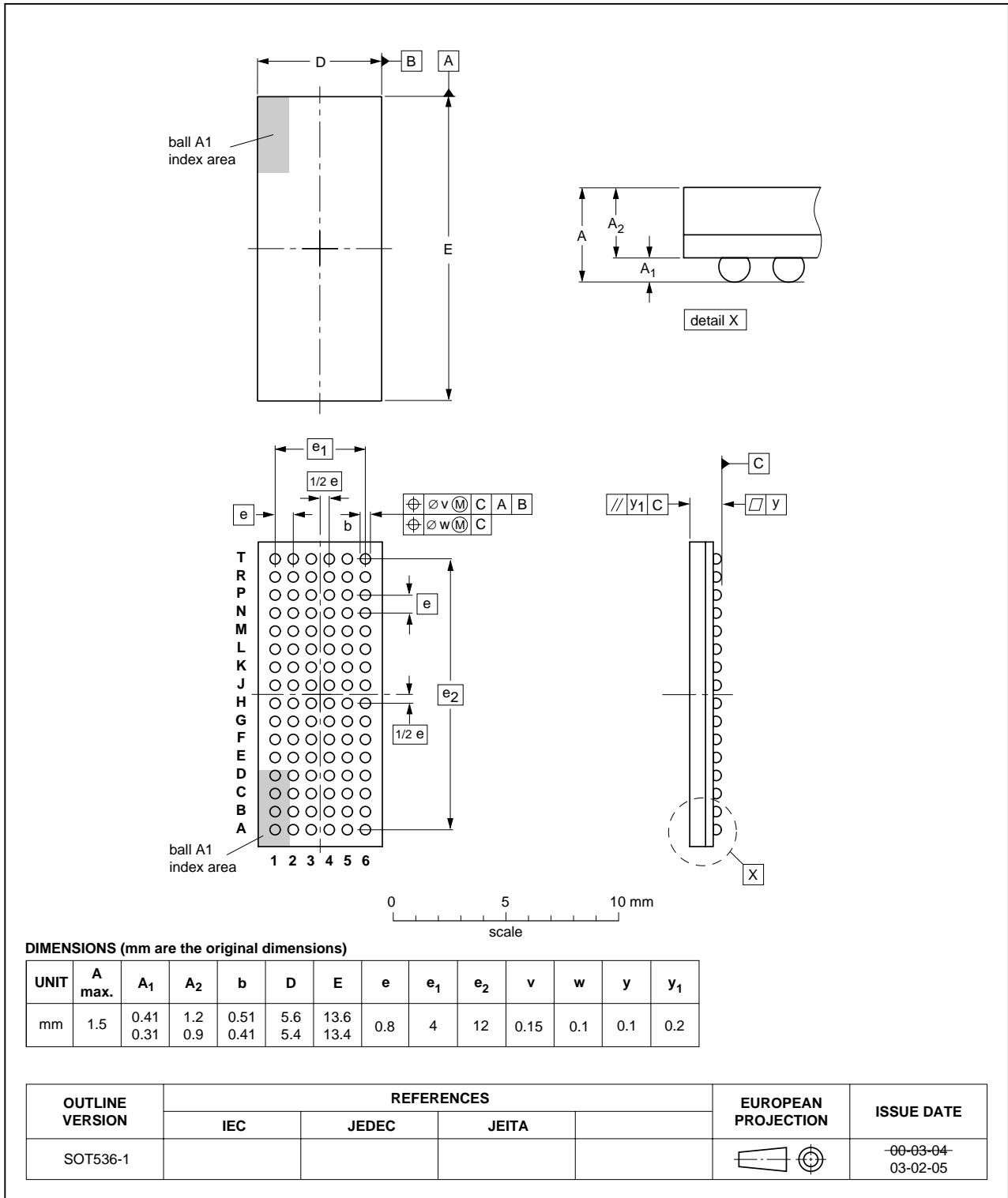


Fig 16. Package outline SOT536-1 (LFBGA96)

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

12.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

| Package [1] | Soldering method | |
|--|-------------------------|--------------|
| | Wave | Reflow [2] |
| BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable [4] | suitable |
| PLCC [5], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended [5] [6] | suitable |
| SSOP, TSSOP, VSO, VSSOP | not recommended [7] | suitable |
| CWQCCN..L [8], PMFP [9], WQCCN..L [8] | not suitable | not suitable |

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

13. Abbreviations

Table 11: Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Silicon |
| DDR | Double Data Rate |
| DIMM | Dual In-line Memory Module |
| JEDEC | Joint Electron Device Engineering Council |
| LFBGA | Low profile Fine-pitch Ball Grid Array |
| LVC MOS | Low Voltage Complementary Metal Oxide Silicon |
| PRR | Pulse Repetition Rate |
| RDIMM | Registered Dual In-line Memory Module |
| SSTL | Stub Series Terminated Logic |

14. Revision history

Table 12: Revision history

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|----------------|---|--------------------|---------------|----------------|--------------|
| SSTU32864_2 | 20041022 | Product data sheet | - | 9397 750 14092 | SSTU32864-01 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Data sheet status changed to 'Product data sheet'. • Table 2 "Pin description" <ul style="list-style-type: none"> – (new) Table note [1] added – pin (ball) numbers added – changed pin name 'DNU' to 'd.n.u.' • Table 3 "Function table (each flip-flop)" <ul style="list-style-type: none"> – moved to Section 6.1 on page 7 – added Table note 1 and its reference at 'Outputs' – corrected column sub-headings under 'Outputs' • Table 4 "Limiting values [1]": Symbol V_i changed to V_I; Symbol V_o changed to V_O • Table 5 "Operating conditions": <ul style="list-style-type: none"> – changed V_{IH} (for data inputs) to $V_{IH(AC)}$ and $V_{IH(DC)}$; condition changed to 'data inputs (Dn)' – changed V_{IL} (for data inputs) to $V_{IL(AC)}$ and $V_{IL(DC)}$; condition changed to 'data inputs (Dn)' – Table note split into 2 notes; references added. • Table 6 "Characteristics" <ul style="list-style-type: none"> – changed I_{DDP} Parameter from "dynamic operating current ..." to "dynamic operating current per MHz ..."; change Unit from "$\mu A/MHz$" to "μA". • Table 7 "Timing requirements": <ul style="list-style-type: none"> – changed symbol f_{CLOCK} to f_{clock} – changed symbol t_{SU} to t_{su} – changed symbol t_H to t_h • Table 8 "Switching characteristics": <ul style="list-style-type: none"> – changed t_{PDM} and t_{PDMSS} Conditions from 'clock to output' to 'CK and \overline{CK} to output' – changed t_{PHL} Condition from 'reset to output' to '\overline{RESET} to output' • Table 9 "Output edge rates": deleted Table note [1] • Section 10.1 "Test circuit": titles for Figure 10 and Figure 11 modified. • Added Section 13 "Abbreviations" | | | | |
| SSTU32864-01 | 20040712 | Objective data | - | 9397 750 13339 | - |

15. Data sheet status

| Level | Data sheet status ^[1] | Product status ^[2] ^[3] | Definition |
|-------|----------------------------------|--|--|
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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19. Contents

| | | |
|-----------|--|-----------|
| 1 | General description | 1 |
| 2 | Features | 2 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 3 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 6 |
| 6 | Functional description | 7 |
| 6.1 | Function table | 7 |
| 7 | Limiting values | 8 |
| 8 | Recommended operating conditions | 9 |
| 9 | Characteristics | 10 |
| 10 | Test information | 12 |
| 10.1 | Test circuit | 12 |
| 10.2 | Output slew rate measurement | 14 |
| 11 | Package outline | 15 |
| 12 | Soldering | 16 |
| 12.1 | Introduction to soldering surface mount packages | 16 |
| 12.2 | Reflow soldering | 16 |
| 12.3 | Wave soldering | 16 |
| 12.4 | Manual soldering | 17 |
| 12.5 | Package related soldering information | 17 |
| 13 | Abbreviations | 18 |
| 14 | Revision history | 19 |
| 15 | Data sheet status | 20 |
| 16 | Definitions | 20 |
| 17 | Disclaimers | 20 |
| 18 | Contact information | 20 |



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