PIC16F785/HV785

PIC16F785/HV785
Silicon Errata and Data Sheet Clarification

The PIC16F785/HV785 device that you have received conform functionally to the current Device Data Sheet (DS41249**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F785/HV785.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision.

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16F785/HV785 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A2	A3
PIC16F785	`01 0010 001x xxxx`	2	3
PIC16HV785	`01 0010 000x xxxx`	2	3

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16F785/HV785 Memory Programming Specification"* (DS41237) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY PIC16F785/HV785

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A2	A3
Two-Phase PWM	Complementary Mode	1.	Complementary Mode	X	X
Two-Phase PWM	Two-Phase PWM	2.	PWM may freeze on shut-down	X	X
Capture/Compare/PWM	Capture	3.	First capture may happen early	X	X
Capture/Compare/PWM	I/O	4.	Pin RC5 reads low	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Two-Phase PWM (Complementary Mode)

The Complementary mode is not supported due to the nature and extent of the Complementary mode anomalies. Complementary mode should be used for evaluation purposes only.

1. Duty cycle by comparator feedback (COMOD = X1) is not supported.
2. When the duty cycle is determined by the difference between the PH1 and PH2 phase delays (CMOD = `10`), both outputs can sometimes hang low if the duty cycle is less than 20 ns or greater than the phase switching dead time. The hang condition can only be cleared by setting the dead time to zero.
3. Maximum phase switching dead time is limited by the PWM clock frequency (`pwm_clock`). At a `pwm_clock` frequency of 20 MHz, the maximum dead time is about 35 ns. At a `pwm_clock` frequency of 10 MHz, the maximum dead time is about 80 ns. The relationship between maximum dead time and `pwm_clock` frequency is approximately linear.
4. The shutdown condition will correctly force PH1 false (low output at PH1 flop before the inverting XOR gate). PH2 will be incorrectly forced true (high output at PH2 flop before inverting XOR gate).
5. If the dead time is not zero and PWMPH1<4:0> = PWMPH2<4:0> then both phase outputs will be driven false (PH1 and PH2 low before inverting XOR gate). If the dead time is zero and PWMPH1<4:0> = PWMPH2<4:0>, then phase 1 will be driven true (PH2 high) for all but one `pwm_clock` cycles every PWM period.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

2. Module: Two-Phase PWM (Two-Phase Mode)

1. If the PWMASE bit is set when the PASEN bit is cleared, then the PWMASE bit will be stuck high and the PWM will be frozen in shutdown. Shutdown can only be cleared by first setting the PASEN bit high then clearing the shutdown condition (RA2/INT input must be high) so the PWMASE bit can be cleared.
2. In normal two-phase operation when the output is inverted, the leading edge is delayed by about 10 ns and the trailing edge occurs about 7 ns early. When the phase delay is set to maximum, the leading edge is delayed about 8 ns. The net result of these two phenomena is that at 20 MHz FOSC, a blanked inverted output at maximum phase delay will not be generated.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

3. Module: Capture/Compare/PWM (CCP)

The first capture will occur one edge too early if the RC5/CCP1 input is high when selecting the CCP mode to capture either every 4th edge (CCP1CON<3:0> = `0110`) or every 16th edge (CCP1CON<3:0> = `0111`). Subsequent captures will occur properly.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

4. Module: Capture/Compare/PWM (CCP)

Reading bit 5 of PORTC (RC5/CCP1) always returns a '0' when the CCP module is configured for any of the four capture modes (CCP1CON<3:0> = 01XX). This condition is true when the RC5/CCP1 pin is configured as either an input (TRISC<5> = 1) or output (TRISC<5> = 0). When configured as an output, the ability to set the RC5/CCP1 pin high or low works normally although reading the pin status always returns '0'.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41249**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

Corrections to Table 19-15, Param. No. A20/A20A.

TABLE 19-15: PIC16F785/HV785 A/D CONVERTER CHARACTERISTICS:

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	
A03	EIL	Integral Error	—	—	±1	LSb	VREF = 5.0V (external)
A04	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.0V (external)
A06	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.0V (external)
A07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.0V (external)
A20	VREF	Reference Voltage	2.2**(4)**	—	**VDD**	V	
A20A			2.5	—	**VDD**	V	Absolute minimum to ensure 1 LSB accuracy.
A25	VAIN	Analog Input Voltage	VSS	—	VREF**(5)**	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	IREF	VREF Input Current***(3)**	10 —	— —	1000 50	μA μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. Transient during A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes Integral, Differential, Offset and Gain Errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: VREF current is from external VREF or VDD pin, whichever is selected as reference input.

4: Only limited when VDD is at or below 2.5V. If VDD is above 2.5V, VREF is allowed to go as low as 1.0V.

5: Analog input voltages are allowed up to VDD, however the conversion accuracy is limited to VSS to VREF.

2. Module: A/D Converter

Corrections to Equation 12-1.

EQUATION 12-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$
\begin{aligned}
T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
&= T_{AMP} + T_C + T_{COFF} \\
&= 5\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]
\end{aligned}
$$

The value for Tc can be approximated with the following equations:

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \quad \text{;[1] Vchold charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad \text{;[2] Vchold charge response to Vapplied}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \quad \text{;Combining [1] and [2]}$$

Solving for Tc:

$$
\begin{aligned}
T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047) \\
&= -12pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885) \\
&= 1.64\mu s
\end{aligned}
$$

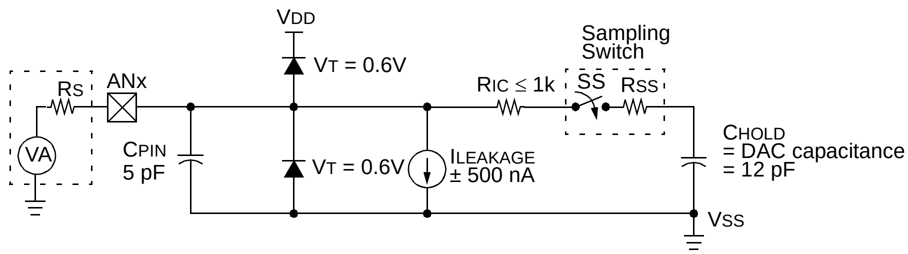
Therefore:

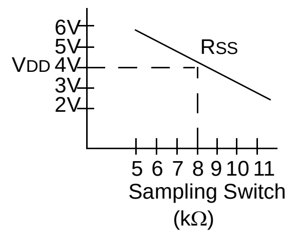
$$
\begin{aligned}
T_{ACQ} &= 5\mu s + 1.64\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\
&= 7.89\mu s
\end{aligned}
$$

3. Module: A/D Converter

Corrections to Figure 12-4.

FIGURE 12-4: ANALOG INPUT MODEL





Legend:

CPIN =	Input Capacitance
VT =	Threshold Voltage
I LEAKAGE =	Leakage current at the pin due to various junctions
RIC =	Interconnect Resistance
SS =	Sampling Switch
CHOLD =	Sample/Hold Capacitance (from DAC)

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2007)

First release of document. Added Module 1, "Two-Phase PWM" and Module 2, "Two-Phase Mode".

Rev B Document (5/2005)
Added item #5 and #6 to Module 1, "Two-Phase PWM (Complementary mode)".

Rev C Document (7/2005)
Clarifications/Corrections to the Data Sheet:
Added Module 1, New 4x4 QFN Package added.

Rev D Document (12/2005)

Added Modules 3 and 4, "Capture/Compare/PWM (CCP)".

Rev E Document (08/2009)

Updated document to new format. Updated Table 1 and Table 2.

Data Sheet Clarifications: Deleted Module 1: New 4x4 QFN Package; Added Module 1: Electrical Characteristics (Table 19-15); Added Module 2: A/D Converter (Equation 12-1); Added Module 3: A/D Converter (Figure 12-4).

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