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Kind regards,

Team Nexperia

74CBTLVD3244

8-bit level-shifting bus switch with 4-bit output enables

Rev. 2 — 16 December 2011 Product data sheet

1. General description

The 74CBTLVD3244 is a dual 4-pole, single-throw bus switch. The device features two output enable inputs ($n\overline{OE}$) that each control four switch channels. The switches are disabled when the associated $n\overline{OE}$ input is HIGH. Schmitt trigger action at control inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLVD3244DS	–40 °C to +125 °C	SSOP20[1]	plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT724-1
74CBTLVD3244PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74CBTLVD3244BQ	–40 °C to +125 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

[1] Also known as QSOP20 package

4. Functional diagram

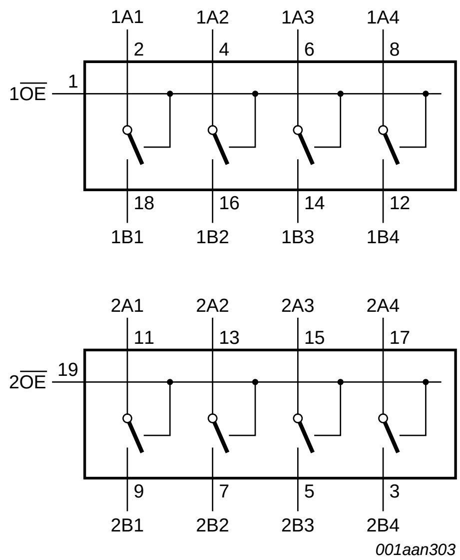


Fig 1. Logic symbol

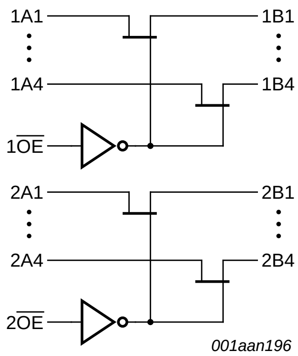


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

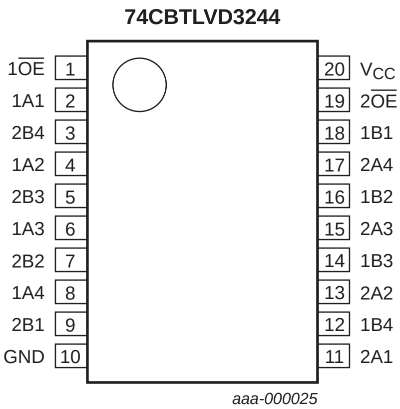


Fig 3. Pin configuration for TSSOP20 (SOT360-1)

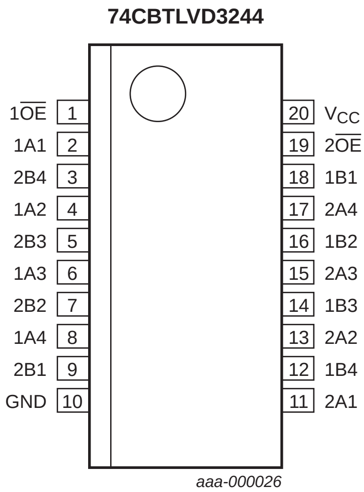
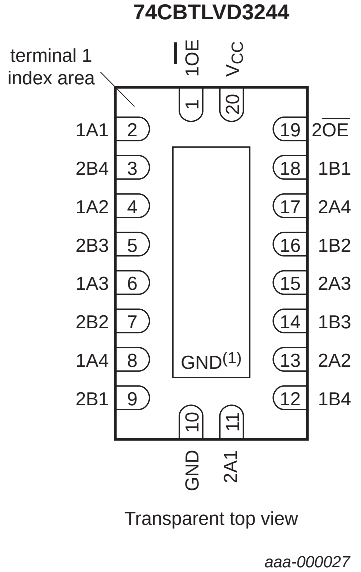


Fig 4. Pin configuration for SSOP20 (SOT724-1)



(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN20 (SOT764-1)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 19	output enable input (active LOW)
1A1 to 1A4	2, 4, 6, 8	data input/output (A port)
2B1 to 2B4	9, 7, 5, 3	data input/output (A port)
GND	10	ground (0 V)
2A1 to 2A4	11, 13, 15, 17	data input/output (B port)
1B1 to 1B4	18, 16, 14, 12	data input/output (B port)
V_{CC}	20	positive supply voltage

6. Functional description

Table 3. Function selection[1]

Input	Input/output
$n\overline{OE}$	**nAn, nBn**
L	nAn = nBn
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode	[1]	–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	$V_{I/O}$ < –0.5 V		–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V		–50	-	mA
I_{SW}	switch current	V_{SW} = 0 V to V_{CC}		-	±128	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SSOP20 and TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			3.0	3.6	V
V_I	input voltage			0	3.6	V
V_{SW}	switch voltage	enable and disable mode		0	V_{CC}	V
T_{amb}	ambient temperature			–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	[1]	0	200	ns/V

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I_I	input leakage current	pin $n\overline{OE}$; V_I = GND to V_{CC}; V_{CC} = 3.6 V	-	-	±1	-	±20	μA
V_{pass}	pass voltage	V_I = V_{CC}; see Figure 8 to Figure 12	-	-	-	-	-	V

Table 6. Static characteristics *...continued*

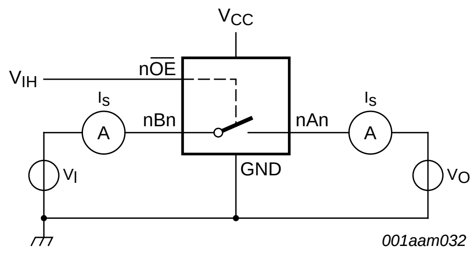
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 3.6 V; see Figure 6		-	-	±1	-	±20	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 3.6 V; see Figure 7		-	-	±1	-	±20	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±10	-	±50	μA
I_{CC}	supply current	$V_I = V_{CC}$; I_O = 0 A; V_{CC} = 3.6 V; V_{SW} = GND or V_{CC}		-	-	20	-	50	μA
		V_I = GND; I_O = 0 A; V_{CC} = 3.6 V; V_{SW} = GND or V_{CC}		-	-	100	-	150	μA
ΔI_{CC}	additional supply current	pin $n\overline{OE}$; $V_I = V_{CC} - 0.6$ V; V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V	[2]	-	-	300	-	2000	μA
C_I	input capacitance	pin $n\overline{OE}$; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V		-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V		-	2.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	V_{CC} = 3.3 V; V_I = 0 V to 3.3 V		-	9.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

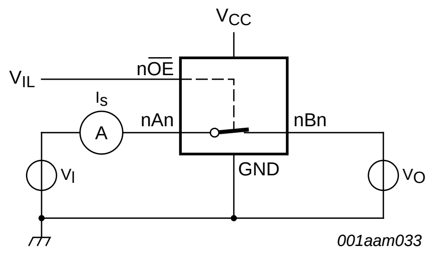
[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1 Test circuits



$V_I = V_{CC}$ or GND and V_O = GND or V_{CC}.

Fig 6. Test circuit for measuring OFF-state leakage current (one switch)



$V_I = V_{CC}$ or GND and V_O = open circuit.

Fig 7. Test circuit for measuring ON-state leakage current (one switch)

9.2 Typical pass voltage graphs

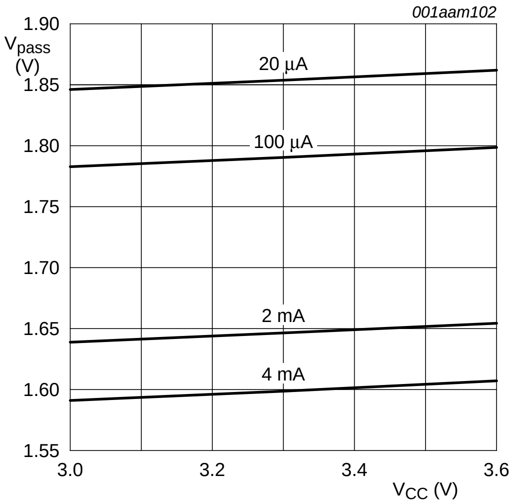


Fig 8. Pass voltage versus supply voltage; T_{amb} = 125 °C (typical)

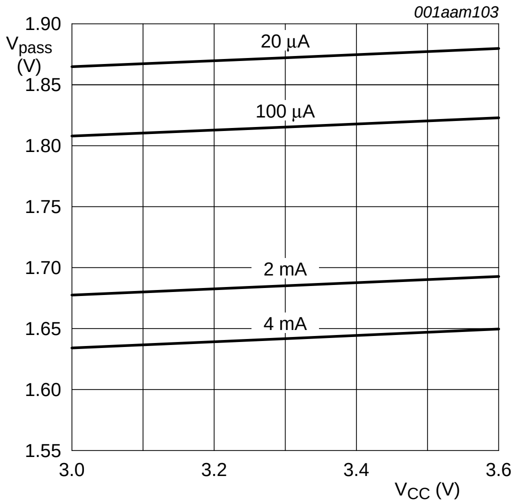


Fig 9. Pass voltage versus supply voltage; T_{amb} = 85 °C (typical)

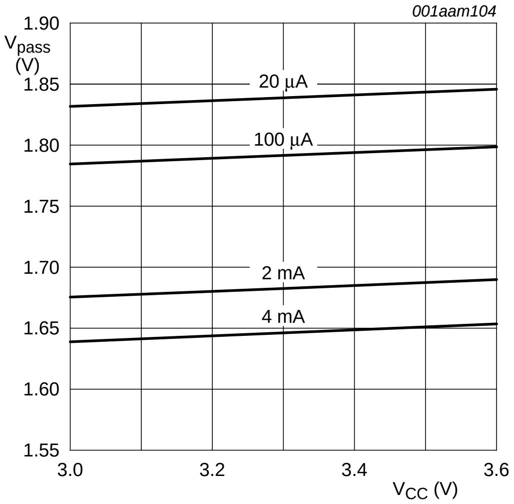


Fig 10. Pass voltage versus supply voltage; T_{amb} = 25 °C (typical)

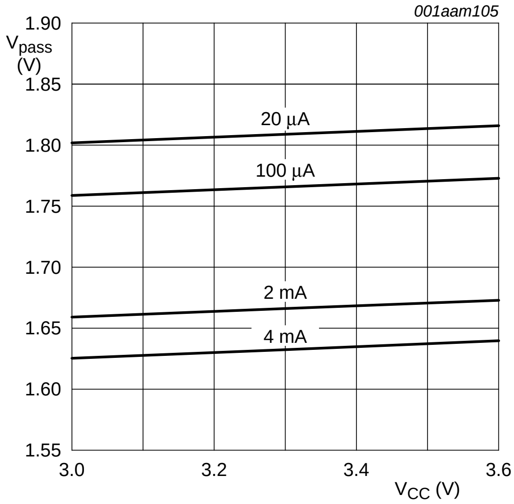


Fig 11. Pass voltage versus supply voltage; T_{amb} = 0 °C (typical)

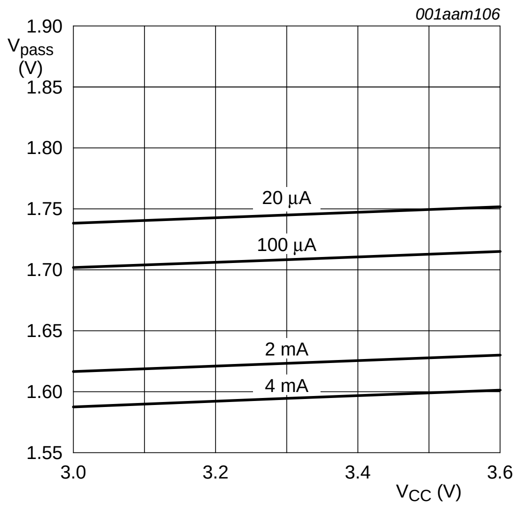


Fig 12. Pass voltage versus supply voltage; T_{amb} = –40 °C (typical)

9.3 ON resistance

Table 7. Resistance R_{ON}

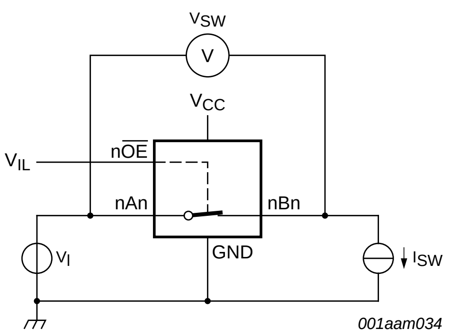
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R_{ON}	ON resistance	V_{CC} = 3.0 V to 3.6 V						
		I_{SW} = 64 mA; V_I = 0 V	-	3.7	7.0	-	10.0	Ω
		I_{SW} = 24 mA; V_I = 0 V	-	3.7	7.0	-	10.0	Ω
		I_{SW} = 15 mA; V_I = 1.2 V	-	4.7	10.0	-	12.0	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.4 ON resistance test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig 13. Test circuit for measuring ON resistance (one switch)

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Figure 16

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nAn to nBn or nBn to nAn; see Figure 14	[2][3]						
		V_{CC} = 3.0 V to 3.6 V		-	-	0.11	-	0.22	ns
t_{en}	enable time	$n\overline{OE}$ to nAn or nBn; see Figure 15	[4]						
		V_{CC} = 3.0 V to 3.6 V		1.5	2.8	5.0	1.5	6.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn or nBn; see Figure 15	[5]						
		V_{CC} = 3.0 V to 3.6 V		0.8	3.1	7.0	0.8	8.0	ns

[1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.

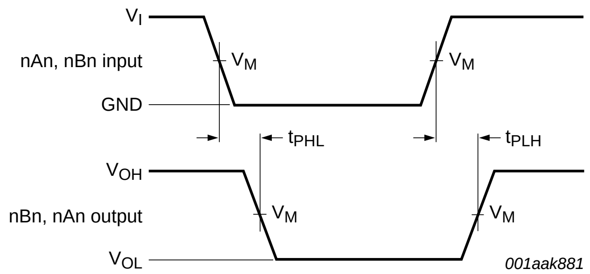
[2] The propagation delay is the calculated RC time constant of the on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

11. Waveforms



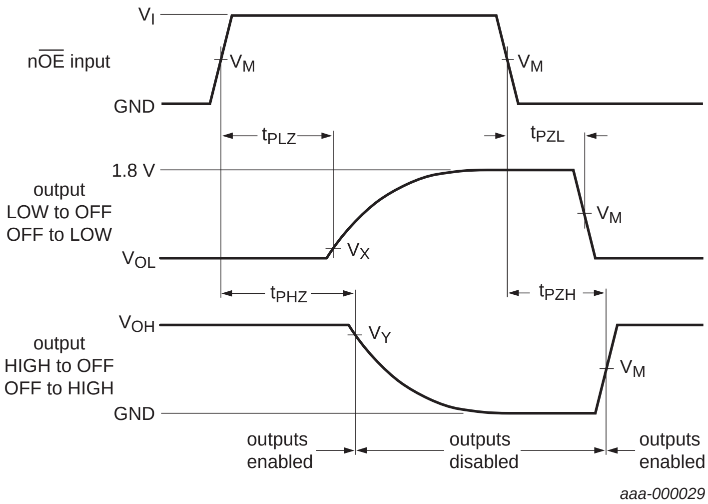
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times

Table 9. Measurement points

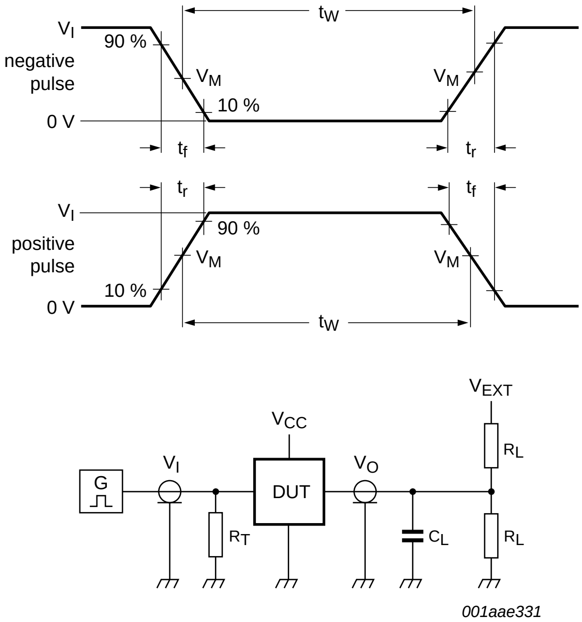
Supply voltage	Input			Output		
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	0.9 V	V_{OL} + 0.15 V	V_{OH} − 0.15 V



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 15. Enable and disable times



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V to 3.6 V	30 pF	1 kΩ	open	GND	3.6 V

11.1 Additional dynamic characteristics

Table 11. Additional dynamic characteristics

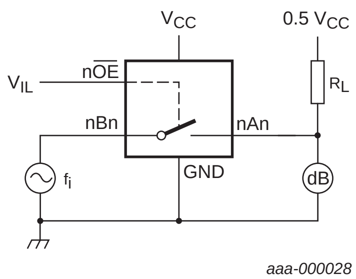
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			Unit
				Min	Typ	Max	
$f_{(-3dB)}$	−3 dB frequency response	V_{CC} = 3.3 V; R_L = 50 Ω; see Figure 17	[2]	-	575	-	MHz

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

[2] f_i is biased at $0.5V_{CC}$.

11.2 Test circuits

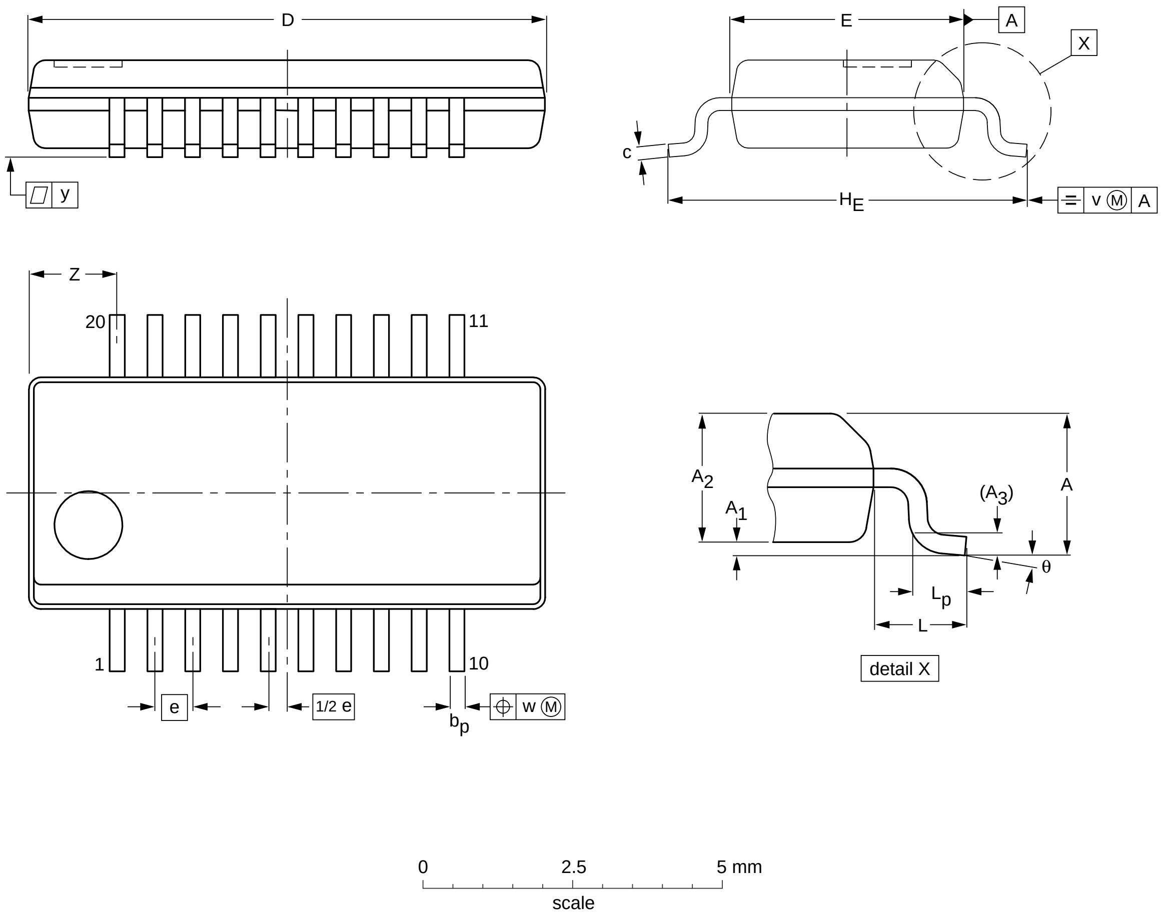


$n\overline{OE}$ connected to GND; Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Fig 17. Test circuit for measuring the frequency response when channel is in ON-state

12. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT724-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	8.8 8.6	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.25	0.18	0.1	1.67 1.28	8^o 0^o

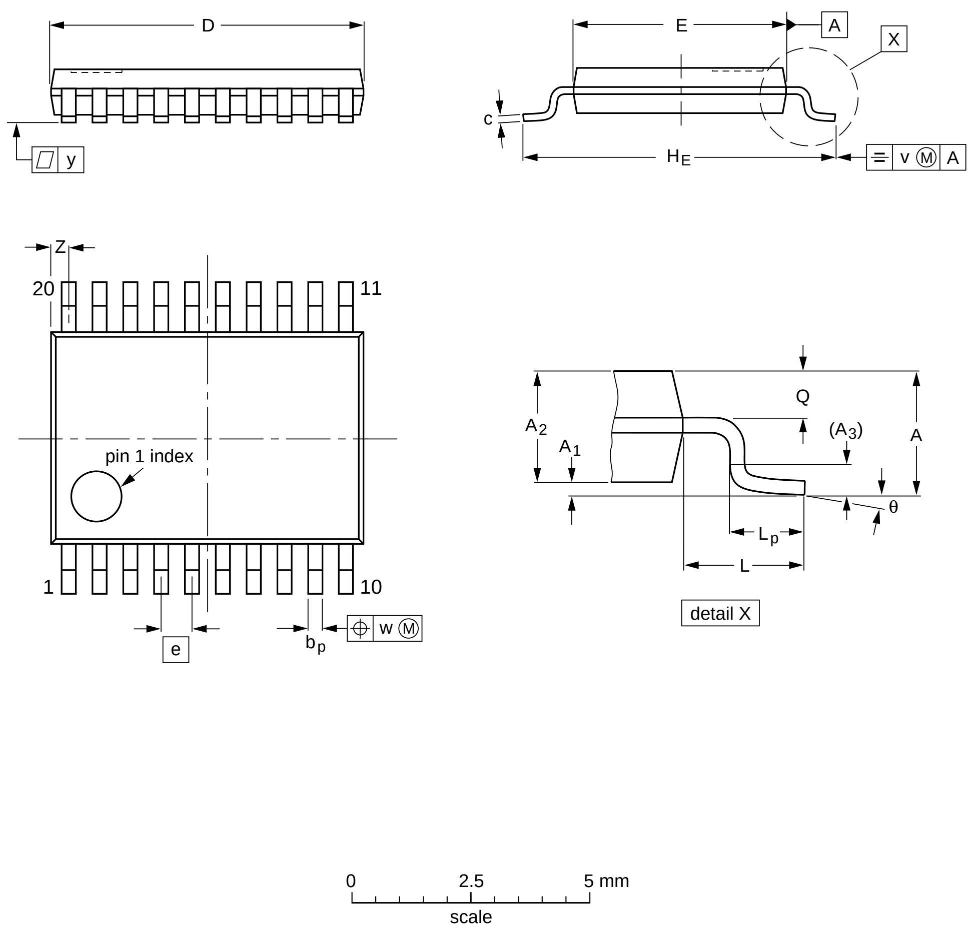
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT724-1		MO-137				~~01-07-04~~ 03-02-18

Fig 18. Package outline SOT724-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

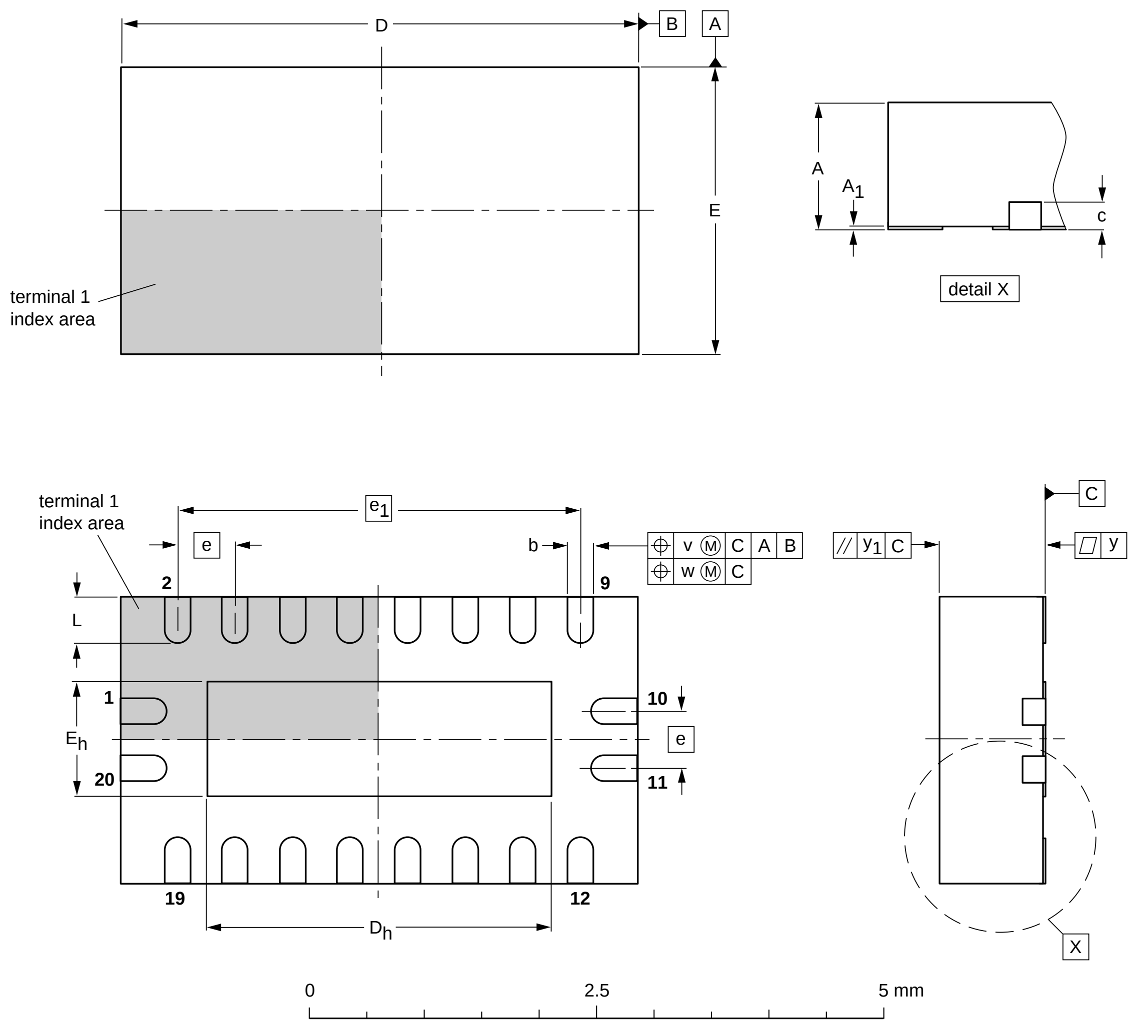
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 20. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLVD3244 v.2	20111216	Product data sheet	-	74CBTLVD3244 v.1
Modifications:	• Legal pages updated.			
74CBTLVD3244 v.1	20110715	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

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