SiM3U167-B-GDI

High-Performance, Low-Power, 32-Bit Precision32™ USB MCU Family with up to 256 kB of Flash Die in Wafer Form

32-bit ARM® Cortex™-M3 CPU

- 80 MHz maximum frequency
- Single-cycle multiplication, hardware division support
- Nested vectored interrupt control (NVIC) with 16 priority levels

Memory

- 32–256 kB Flash, in-system programmable
- 8–32 kB SRAM (including 4 kB retention SRAM)
- 16-channel DMA controller
- External bus interface supports up to 16 MB of external memory and a parallel LCD interface with QVGA resolution

Power Management

- Low drop-out (LDO) regulator
- Power-on reset circuit and brownout detectors
- 5–3.3 V 150 mA regulator supports direct USB power
- Adjustable external regulator supports up to 3.6 V, 1000 mA
- Multiple power modes supported for low power optimization

Low Power Features

- 85 nA current mode with voltage supply monitor enabled
- Low-current RTC: 350 nA internal LFO, 620 nA external crystal
- 10 µs wakeup (lowest power mode); 1.5 µs analog setting time
- 275 µA/MHz active current
- Clocks can be gated off from unused peripherals to save power
- Flexible clock divider: Reduce operational frequency up to 128x

Clock Sources

- Internal oscillator with PLL: 23-80 MHz, reduced EMI mode
- USB internal 48 MHz oscillator supports crystal-less operation
- Low power internal oscillator: 20 MHz and 2.5 MHz modes
- Low frequency internal oscillator: 16.4 kHz
- External oscillators: Crystal, RC, C, CMOS and RTC Crystal

Supply Voltage

- 2.7 to 5.5 V (regulator enabled)
- 1.8 to 3.6 V (regulator disabled)

Temperature Range: –40 to +85 °C

Analog Peripherals

- 2 x 12-Bit Analog-to-Digital Converters: Up to 250 ksps 12-bit mode or 1 Msps 10-bit mode, internal or external reference
- 2 x 10-Bit Current-mode Digital-to-Analog Converters, four-word buffer enables 12-bit operation
- 2 x Low-current comparators
- 16-Channel Capacitance-to-Digital: Fast, <1 µA wake-on-touch
- 2 x Current-to-Voltage Converter, up to 6 mA input range

Digital and Communication Peripherals

- USB 2.0-compliant full speed with 10 endpoints, 2 kB buffer, oscillator with automatic frequency correction, and transceiver; no external components needed
- 2 x USARTs and 2 x UARTs with IrDA and ISO7816 SmartCard
- 3 x SPIs, 2 x I2C, I^2S (receive and transmit), 16/32-bit CRC
- 128/192/256-bit Hardware AES Encryption

Timers/Counters

- 2 x 32-bit or 4 x 16-bit timers with capture/compare
- 2 x 16-bit, 2-channel counters with capture/compare/PWM
- 16-bit, 6-channel counter with capture/compare/PWM and dead-time controller with differential outputs
- 16-bit low power timer/pulse counter operational in sleep
- 32-bit real time clock (RTC) with multiple alarms
- Watchdog timer

Up to 65 Flexible I/O

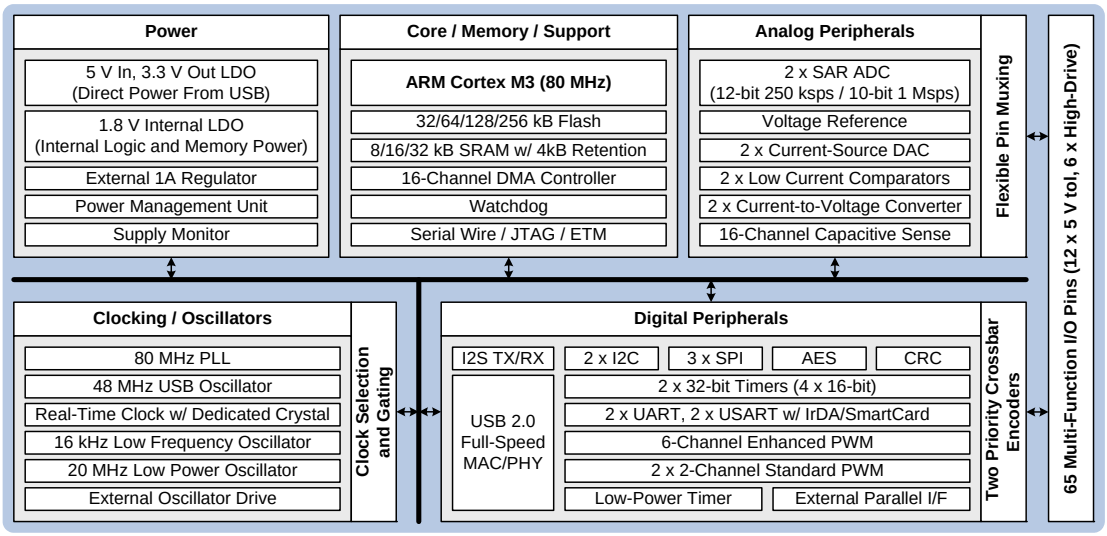
- Up to 59 contiguous GPIO with two priority crossbars providing flexibility in pin assignments; 12 x 5 V tolerant GPIO
- Up to 6 programmable high drive capable (5–300 mA, 1.8–6 V) I/O can drive LEDs, power MOSFETs, buzzers, etc.

On-Chip Debugging

- Serial wire debug (SWD) or JTAG (no boundary scan), serial wire viewer (SWV)
- Cortex-M3 embedded trace macrocell (ETM)

Full Technical Data Sheet

- SiM3U1xx



1. Ordering Information

Table 1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (kB)	External Memory Interface (EMIF)	Maximum Number of EMIF Address/Data Pins	Digital Port I/Os (Total)	Digital Port I/Os with High Drive Capability	Number of SARADC0 Channels	Number of SARADC1 Channels	Number of CAPSENSE0 Channels	Number of Comparator 0/1 Inputs (+/-)	Number of PMU Pin Wake Sources	JTAG Debugging Interface	ETM Debugging Interface	Serial Wire Debugging Interface	Wafer Thickness
SiM3U167-B-GDI	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	12 mil backgrind
SiM3U167-B-G1DI	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	28.54 mil/725 µm (no backgrind)

2. Pin Definitions

Table 2 lists the pin definitions for the SiM3U167-GDI. For a full description of each pin, refer to the SiM3U1xx data sheet.

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB4.5	High Drive I/O	1				LSO5			
PB4.4	High Drive I/O	2				LSO4			
PB4.3	High Drive I/O	3				LSO3			
VSSHD	Ground (High Drive)	4							
VIOHD	Power (High Drive)	5							
PB4.2	High Drive I/O	6				LSO2			
PB4.1	High Drive I/O	7				LSO1			
PB4.0	High Drive I/O	8				LSO0			
VSS	Ground	9							
Reserved*	No Connect	10							
Reserved*	No Connect	11							
Reserved*	No Connect	12							
PB3.11	5 V Tolerant I/O	13	XBR1	✓				WAKE.15	CMP0N.7 CMP1N.7 EXREGBD
PB3.10	5 V Tolerant I/O	14	XBR1	✓				INT0.15 INT1.15 WAKE.14	CMP0P.7 CMP1P.7 EXREGOUT
PB3.9	5 V Tolerant I/O	15	XBR1	✓	$\overline{\text{BE0}}$			DAC0T6 DAC1T6 INT0.14 INT1.14 WAKE.13	CMP0N.6 CMP1N.6 EXREGSN

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI (Continued)

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.8	5 V Tolerant I/O	16	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T2 INT0.13 INT1.13 WAKE.12	CMP0P.6 CMP1P.6 EXREGSP
PB3.7	5 V Tolerant I/O	17	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 LPT0T1 INT0.12 INT1.12 WAKE.11	CMP0N.5 CMP1N.5
PB3.6	5 V Tolerant I/O	18	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.11 INT1.11 WAKE.10	CMP0P.5 CMP1P.5
VSS	Ground	19							
PB3.5	5 V Tolerant I/O	20	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.10 INT1.10 WAKE.9	CMP0N.4 CMP1N.4
PB3.4	5 V Tolerant I/O	21	XBR1	✓	$\overline{OE}$			INT0.9 INT1.9 WAKE.8	CMP0P.4 CMP1P.4
PB3.3	5 V Tolerant I/O	22	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.8 INT1.8	CMP0N.3 CMP1N.3
PB3.2	5 V Tolerant I/O	23	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0	CMP0P.3 CMP1P.3
PB3.1	5 V Tolerant I/O	24	XBR1	✓	AD1m/ D1				CMP0N.2 CMP1N.2

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI (Continued)

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.0	5 V Tolerant I/O	25	XBR1	✓	AD2m/ D2				CMP0P.2 CMP1P.2
PB2.14	Standard I/O	26	XBR1	✓	AD3m/ D3		Yes		CMP0N.1 CMP1N.1
PB2.13	Standard I/O	27	XBR1	✓	AD4m/ D4		Yes		CMP0P.1 CMP1P.1
PB2.12	Standard I/O	28	XBR1	✓	AD5m/ D5		Yes		CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.11	Standard I/O	29	XBR1	✓	AD6m/ D6		Yes		CMP0P.0 CMP1P.0
PB2.10	Standard I/O	30	XBR1	✓	AD7m/ D7		Yes		
PB2.9	Standard I/O	31	XBR1	✓	AD8m/ A0		Yes		
PB2.8	Standard I/O	32	XBR1	✓	AD9m/ A1		Yes		
PB2.7	Standard I/O	33	XBR1	✓	AD10m/ A2		Yes	INT0.7 INT1.7	
PB2.6	Standard I/O	34	XBR1	✓	AD11m/ A3		Yes	INT0.6 INT1.6	
PB2.5	Standard I/O	35	XBR1	✓	AD12m / A4	LSI5	Yes	INT0.5 INT1.5	
PB2.4	Standard I/O	36	XBR1	✓	AD13m/ A5	LSI4	Yes	INT0.4 INT1.4 WAKE.7	
VIO	Power (I/O)	37							
VSS	Ground	38							
VSS	Ground	39							

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI (Continued)

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB2.3	Standard I/O	40	XBR1	✓	AD14m/ A6	LSI3	Yes	INT0.3 INT1.3 WAKE.6	
PB2.2	Standard I/O	41	XBR1	✓	AD15m/ A7	LSI2	Yes	INT0.2 INT1.2 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB2.1	Standard I/O	42	XBR1	✓	A16m/ A8	LSI1	Yes	INT0.1 INT1.1 WAKE.4	ADC1.1 CS0.14
PB2.0	Standard I/O	43	XBR1	✓	A17m/ A9	LSI0	Yes	INT0.0 INT1.0 WAKE.3	ADC1.2 CS0.13
PB1.15	Standard I/O	44	XBR0	✓	A18m/ A10			WAKE.2	ADC1.3 CS0.12
VSS	Ground	45							
PB1.14	Standard I/O	46	XBR0	✓	A19m/ A11			ADC1T15 WAKE.1	ADC1.4 CS0.11
PB1.13	Standard I/O	47	XBR0	✓	A20m/ A12			ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.12	Standard I/O	48	XBR0	✓	A21m/ A13				ADC1.6
PB1.11	Standard I/O	49	XBR0	✓	A22m/ A14			DMA0T0	ADC1.7
PB1.10	Standard I/O	50	XBR0	✓	A23m/ A15			DMA0T1	ADC1.8
SWDIO / TMS	Serial Wire / JTAG	51							
SWCLK / TCK	Serial Wire / JTAG	52							
PB1.9/ TRACECLK	Standard I/O /ETM	53	XBR0	✓					ADC1.9
PB1.8/ETM3	Standard I/O /ETM	54	XBR0	✓					ADC1.10 CS0.9

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI (Continued)

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.7/ETM2	Standard I/O /ETM	55	XBR0	✓					ADC1.11 CS0.8
VIO	Power (I/O)	56							
VSS	Ground	57							
Reserved*	No Connect	58							
PB1.6/ETM1	Standard I/O /ETM	59	XBR0	✓					ADC0.15 ADC1.15
PB1.5/ETM0	Standard I/O /ETM	60	XBR0	✓					ADC0.14 ADC1.14
PB1.4/TDI	Standard I/O /JTAG	61	XBR0	✓					ADC0.13 ADC1.13
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	62	XBR0	✓					ADC0.12 ADC1.12
VSS	Ground	63							
PB1.2/TRST	Standard I/O /JTAG	64	XBR0	✓					
PB1.1	Standard I/O	65	XBR0	✓					ADC0.11
PB1.0	Standard I/O	66	XBR0	✓					XTAL2
PB0.15	Standard I/O	67	XBR0	✓					XTAL1
VSS	Ground	68							
PB0.14	Standard I/O	69	XBR0	✓					IDAC1
PB0.13	Standard I/O	70	XBR0	✓					IDAC0
PB0.12	Standard I/O	71	XBR0	✓					ADC0.10 VREF
PB0.11	Standard I/O	72	XBR0	✓					ADC0.9 VREFGND
PB0.10	Standard I/O	73	XBR0	✓					RTC2
PB0.9	Standard I/O	74	XBR0	✓					ADC0.8 RTC1

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI (Continued)

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	75	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.7	Standard I/O	76	XBR0	✓					ADC0.6 CS0.6 IVC0.0
VSS	Ground	77							
PB0.6	Standard I/O	78	XBR0	✓					CS0.5
PB0.5	Standard I/O	79	XBR0	✓					ADC0.5 CS0.4
PB0.4	Standard I/O	80	XBR0	✓					ADC0.4 CS0.3
PB0.3	Standard I/O	81	XBR0	✓					ADC0.3 CS0.2
PB0.2	Standard I/O	82	XBR0	✓					ADC0.2 CS0.1
PB0.1	Standard I/O	83	XBR0	✓					ADC0.1 CS0.0
PB0.0	Standard I/O	84	XBR0	✓					ADC0.0
VIO	Power (I/O)	85							
VDD	Power (Core)	86							
VDD	Power (Core)	87							
VDD	Power (Core)	88							
VSS	Ground	89							
VSS	Ground	90							
VSS	Ground	91							
VREGIN	Power (Regulator)	92							
VBUS	USB Bus Sense	93							

Table 2. Pin Definitions and Alternate Functions for SiM3U167-B-GDI (Continued)

Pin Name	Type	Physical Pad Number	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
D+	USB Data+	94							
D–	USB Data-	95							
$\overline{\text{RESET}}$	Active-low Reset	96							
VSS	Ground	97							

3. Bonding Instructions

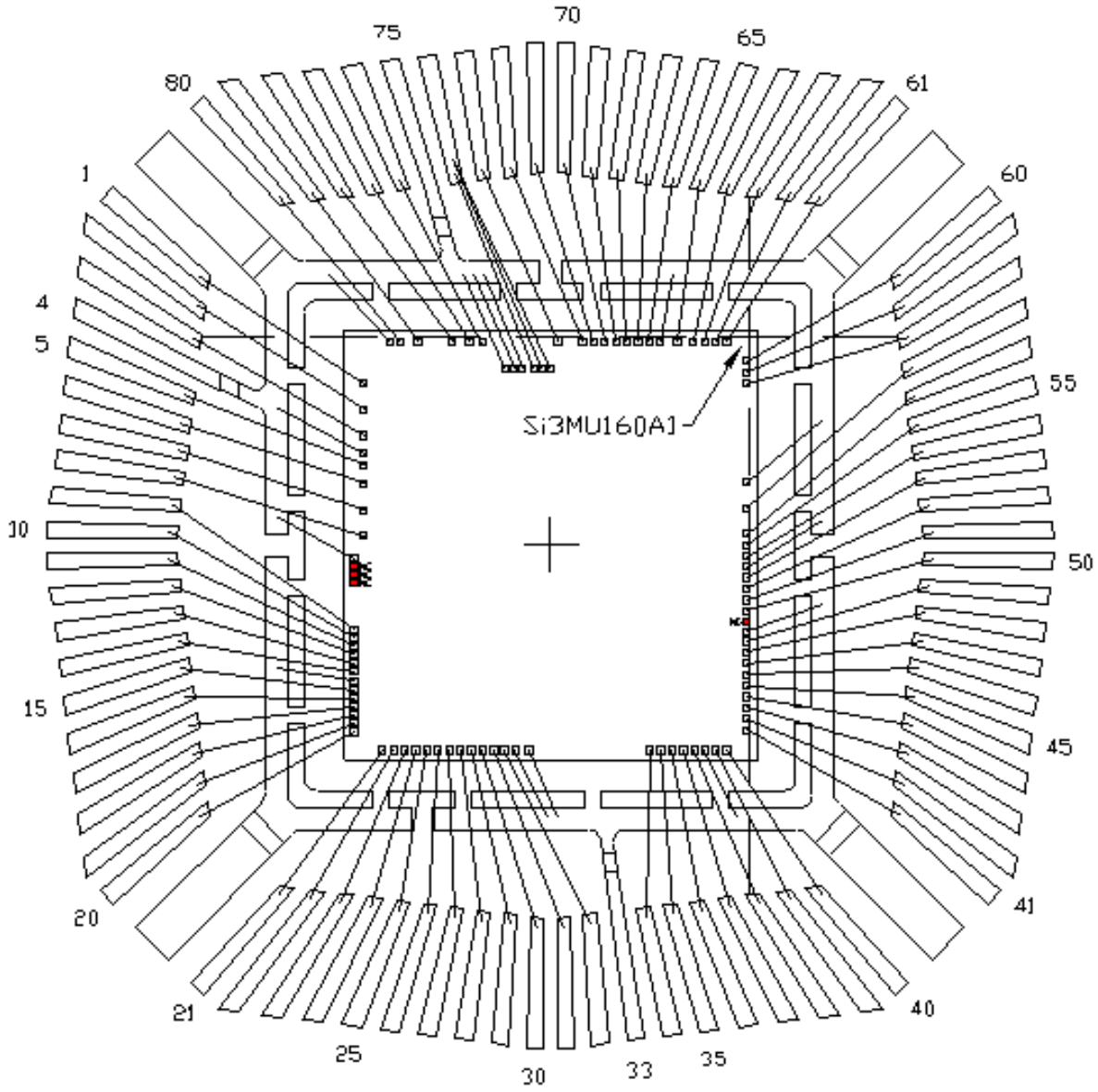


Figure 1. Example Die Bonding (TQFP-80)

Table 3. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (TQFP-80)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
1	1	PB4.5	1674	–1457
2	2	PB4.4	1674	–1224
3	3	PB4.3	1674	–990
4	4	VSSHD	1674	–826
5	5	VIOHD	1674	–721
6	6	PB4.2	1674	–554
7	7	PB4.1	1674	–321
8	8	PB4.0	1674	–87
9	33,75	GND	1760	113
10	NA	Reserved*	1760	188
11	NA	Reserved*	1760	263
12	NA	Reserved*	1760	338
13	9	PB3.11	1760	754
14	10	PB3.10	1760	829
15	11	PB3.9	1760	904
16	12	PB3.8	1760	979
17	13	PB3.7	1760	1054
18	14	PB3.6	1760	1129
19	33,75	GND	1760	1212
20	15	PB3.5	1760	1294
21	16	PB3.4	1760	1369
22	17	PB3.3	1760	1444
23	18	PB3.2	1760	1519
24	19	PB3.1	1760	1594
25	20	PB3.0	1760	1669
26	21	PB2.14	1506	1836

***Note:** Pins marked “Reserved” should not be connected.

Table 3. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (TQFP-80)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
27	22	PB2.13	1406	1836
28	23	PB2.12	1306	1836
29	24	PB2.11	1206	1836
30	25	PB2.10	1106	1836
31	26	PB2.9	1006	1836
32	27	PB2.8	906	1836
33	28	PB2.7	806	1836
34	29	PB2.6	706	1836
35	30	PB2.5	606	1836
36	31	PB2.4	506	1836
37	32	VIO	410	1836
38	33,75	GND	317	1836
39	33,75	GND	190	1836
40	34	PB2.3	–894	1836
41	35	PB2.2	–994	1836
42	36	PB2.1	–1094	1836
43	37	PB2.0	–1194	1836
44	38	PB1.15	–1294	1836
45	33,75	GND	–1390	1836
46	39	PB1.14	–1486	1836
47	40	PB1.13	–1586	1836
48	41	PB1.12	–1765	1657
49	42	PB1.11	–1765	1557
50	43	PB1.10	–1765	1457
51	44	SWDIO/TMS	–1765	1357
52	45	SWCLK/TCK	–1765	1257

***Note:** Pins marked “Reserved” should not be connected.

Table 3. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (TQFP-80)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
53	46	PB1.9/TRACECLK	–1765	1157
54	47	PB1.8/ETM3	–1765	1057
55	48	PB1.7/ETM2	–1765	957
56	49	VIO	–1765	860
57	33,75	GND	–1765	771
58	NA	Reserved*	–1765	680
59	50	PB1.6/ETM1	–1765	587
60	51	PB1.5/ETM0	–1765	487
61	52	PB1.4/TDI	–1765	387
62	53	PB1.3/TDO/SWV	–1765	287
63	33,75	GND	–1765	191
64	54	PB1.2/TRST	–1765	95
65	55	PB1.1	–1765	–5
66	56	PB1.0	–1765	–105
67	57	PB0.15	–1765	–335
68	33,75	GND	–1765	–570
69	58	PB0.14	–1765	–1456
70	59	PB0.13	–1765	–1556
71	60	PB0.12	–1765	–1656
72	61	PB0.11	–1586	–1835
73	62	PB0.10	–1486	–1835
74	63	PB0.9	–1386	–1835
75	64	PB0.8	–1286	–1835
76	65	PB0.7	–1141	–1835
77	33,75	GND	–985	–1835
78	66	PB0.6	–889	–1835

***Note:** Pins marked “Reserved” should not be connected.

Table 3. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (TQFP-80)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
79	67	PB0.5	–789	–1835
80	68	PB0.4	–689	–1835
81	69	PB0.3	–589	–1835
82	70	PB0.2	–489	–1835
83	71	PB0.1	–389	–1835
84	72	PB0.0	–289	–1835
85	73	VIO	–68	–1836
86	74	VDD	–1	–1594
87	74	VDD	74	–1594
88	74	VDD	149	–1594
89	33,75	GND	252	–1594
90	33,75	GND	327	–1594
91	33,75	GND	402	–1594
92	76	VREGIN	607	–1828
93	77	VBUS	724	–1835
94	78	D+	880	–1830
95	79	D–	1190	–1830
96	80	/RESET	1347	–1835
97	33,75	GND	1439	–1835

***Note:** Pins marked “Reserved” should not be connected.

Table 4. Wafer and Die Information

Wafer ID	SiM3U160-B
Wafer Dimensions	8 in
Die Dimensions	3755.64 µm x 3896.6 µm
Wafer Thickness (with backgrind)	12 mil ±1 mil
Wafer Thickness (no backgrind)	28.54 mil ±1 mil (725 µm)
Wafer Identification	Notch
Scribe Line Width	60 µm
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Wafer Specific Information

Known good die are programmed with a value of 0x1C2C5555 at register address 0x40_03E8.

5. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

6. Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet this requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet this requirements will be 3 weeks.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

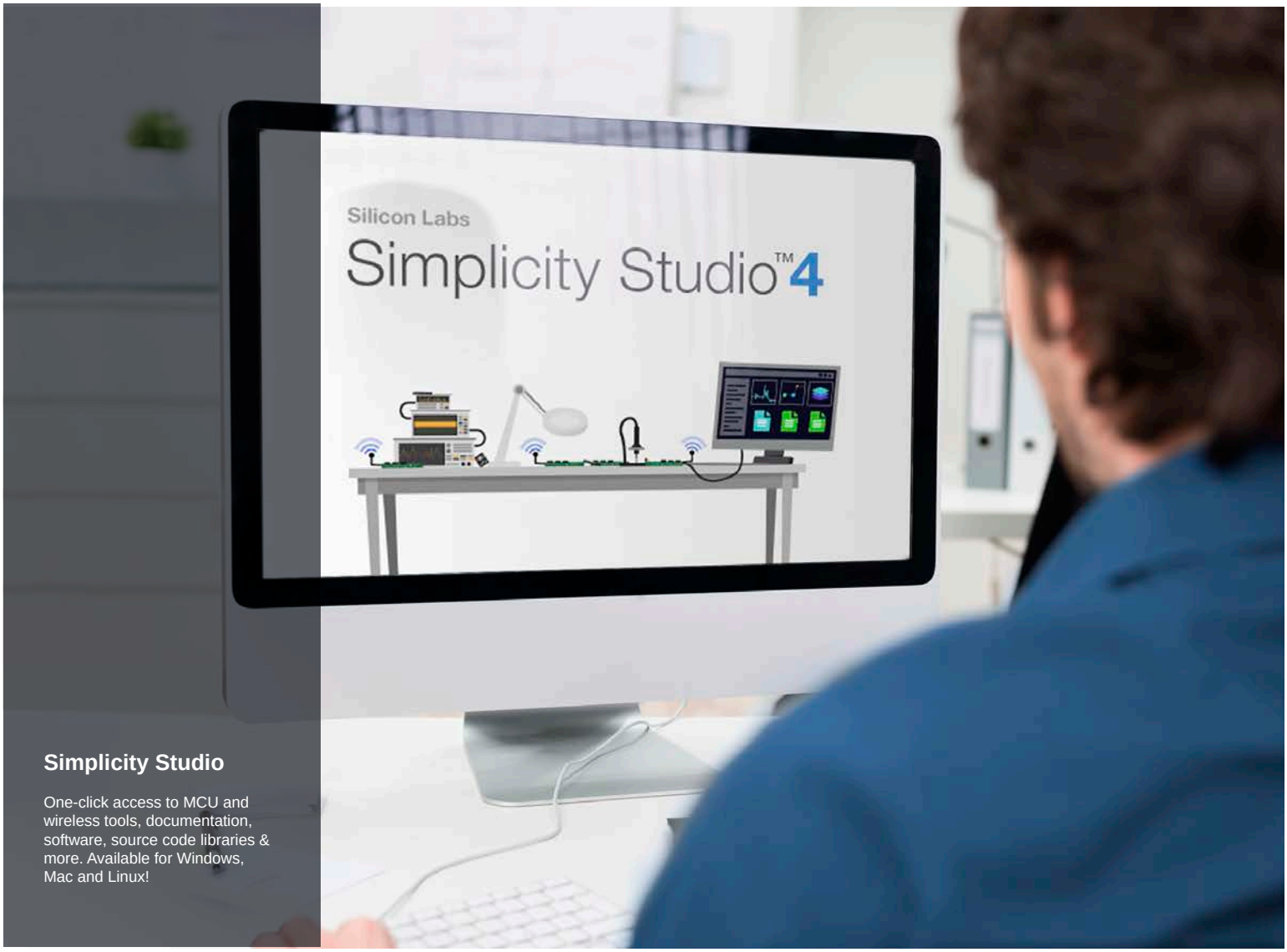
- Updated Table 3 on page 11.
  - Corrected pin name for physical pad number 62.
- Corrected title of Figure 1 on page 10.

Revision 0.2 to Revision 1.0

- Updated front page with block diagram, to match standard device data sheet.
- Updated Table 2 on page 3.
- Changed “RTC0OSC_OUT” pin function to “RTC0TCLK_OUT”.

Revision 1.0 to Revision 1.1

- Added "1. Ordering Information" on page 2.
- Added "2. Pin Definitions" on page 3.
- Added "3. Bonding Instructions" on page 10.
- Updated Table 4, “Wafer and Die Information,” on page 15.
  - Added “backgrind” and “no backgrind” specs.
- Added "4. Wafer Specific Information" on page 16.
- Added "6. Failure Analysis (FA) Guidelines" on page 16.



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