Click here for production status of specific part numbers.

MAX16927

Automotive TFT-LCD Power Supply with Boost, Buck, and Cuk Converters, VCOM Buffers, Gate Drivers, and SPI Interface

General Description

The MAX16927 is a highly integrated power supply for automotive TFT-LCD applications. The device integrates one buck converter, one boost converter, one Cuk converter, two gate-voltage controllers, and two VCOM buffers, one of which supports negative output voltages. The device is designed to operate from a supply voltage between 4.5V and 16V, making it ideal for automotive TFT-LCD applications. Alternatively, the device can operate from an available 3V to 5.5V supply.

The device uses an integrated SPI interface for control and diagnostics. The SPI interface adjusts the VCOM buffer output through an internal 7-bit DAC up to +1V. The startup and shutdown sequences can be controlled through SPI or using one of the three preset stand-alone modes.

The device is optimized for low EMI. Peak interference is reduced by using the spread-spectrum feature. Spread spectrum is always enabled for the buck converter, but enabled through an external input (SSEN) for the boost and Cuk converters. Additional EMI enhancement is achieved by running the boost and Cuk converters 180° out-of-phase.

The device includes a control output for an nMOS switch to enable flexible sequencing of the negative VSL output. A drive output is also included for a series pMOS switch for the boost converter allowing True Shutdown™.

The device is available in a 48-lead TQFN package with an exposed pad, and operates over the -40°C to +105°C temperature range.

Applications

- Automotive Dashboards
- Automotive Central Information Displays
- Automotive Navigation Systems

Benefits and Features

- Operating Voltage Range of 4.5V to 16V (IN3) or 3V to 5.5V (INA)
- 16V Input, 2A Buck Converter Provides 3.3V Output to TFT Bias-Supply Circuitry and/or Other External Circuitry
- Flexible Configuration Allows Single High-Power Positive Output (18V/200mA) or Positive Output (18V, 100mA) and Negative Output (-12V/100mA)
- One Positive Gate-Voltage Regulator
- One Negative Gate-Voltage Controller
- DAC-Controlled VCOM Buffers with Offset of 0V to +1V
- High-Frequency Operation
  - 2.1MHz (Buck Converter)
  - 1.2MHz (Boost and Cuk Converters)
- Converters Run Out-of-Phase for Lower EMI
- Externally Controlled Spread-Spectrum Switching for Boost and Cuk
- Very Flexible Sequencing in Both Stand-Alone and SPI-Controlled Modes
- True Shutdown Boost Converter
- Low-Current Shutdown Mode (< 10µA)
- SPI Control Interface
- Internal Soft-Start
- Overtemperature Shutdown
- -40°C to +105°C Operation
- AEC-Q100 Qualified

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16927GTM/V+	-40°C to +105°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
**EP = Exposed pad.*

***Block Diagram* and *Typical Operating Circuits* appear at end of data sheet.**

True Shutdown is a trademark of Maxim Integrated Products, Inc.

19-5571; Rev 6; 5/18

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Absolute Maximum Ratings

IN3, LXN, LXP, LX3, VCOMP, EN3 to GND.....-0.3V to +20V
BST to GND.....-0.3V to +26V
BST to LX3.....-0.3V to +6V
VCP, VGH to GND.....-0.3V to +24V
DRVN to GND.....-25V to +0.3V
$\overline{FLT}$, INA to GND.....-0.3V to +6V
$\overline{CS}$, CLK, DIN, EN1, EN2, ENP, REF, FBP, FBGH, GATE to GND.....-0.3V to (V_{INA} + 0.3V)
FBGL, FBN, DOUT, SSEN, COMPP, COMPN to GND.....-0.3V to (V_{INA} + 0.3V)
FB3 to GND.....-0.3V to +12V
VCOMH, VCINH to GND.....-0.3V to +20V
VCOML, VCINL to GND (Note 1).....-1.5V to +1.5V
VCOMN to GND.....-7.5V to +0.3V
VCOMP to GND.....-0.3V to +20V
VSLS to GND.....-20V to +0.3V
PGOOD, SYNC, AVL to GND.....-0.3V to +6V
GND to PGND3, PGNDP, PGNDN.....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 38.5mW/°C above +70°C).....3076mW
Operating Temperature Range.....-40°C to +105°C
Junction Temperature Range..... -40°C to +150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: Pin protection is temperature dependent. Temperature behavior T_J = -40°C, ±1.8V; T_J = +150°C, ±0.9V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....26°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN3} = 12V, V_{INA} = 3.3V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BUCK CONVERTER							
Supply Voltage Range	V_{IN3}	V_{OUT} = 3.3V		4.5		16	V
Supply Current	I_{IN3}	V_{EN3} = 0V			10		µA
		V_{EN3} = V_{IN3}, no load			5.3		mA
Undervoltage Lockout (UVLO)		AVL rising			2.7	3	V
		Hysteresis			0.1		
AVL Voltage		6V ≤ V_{IN3} ≤ 16V			5		V
AVL Voltage (Skip Mode)		6V ≤ V_{IN3} ≤ 16V, V_{SYNC} = 0V, I_{LOAD} = 0A			3.3		V
Spread-Spectrum Range					6		%
Switching Frequency	f_{SW}	Internally generated		1.925	2.1	2.275	MHz
SYNC Input Frequency Range				1.8		2.6	MHz
Output Voltage	V_{OUT3}	4.75V ≤ V_{IN3} ≤ 16V, I_{LOAD} < 2A	Continuous mode	3.2%	3.3	3.36%	V
			Skip mode (Note 4)	3.17%	3.3	3.43%	
High-Side DMOS On-Resistance	$R_{DS\_ON(3)}$	I_{LX} = 1000mA, V_{IN3} = V_{AVL} = 5V			100	250	mΩ
DMOS Current-Limit Threshold				2.72	3.4	4.08	A
Soft-Start Ramp Time	t_{SS}			0.25	0.419	0.65	ms
Guaranteed Output Current	$I_{OUT3(MIN)}$	4.75V ≤ V_{IN3} ≤ 16V		2			A
Duty-Cycle Range				15		99	%

Electrical Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD (PGOOD)						
PGOOD Threshold		Rising		92		%
		Falling	88	90	92	
PGOOD Debounce Time				10		µs
PGOOD High-Leakage Current		T_A = +25°C			0.2	µA
PGOOD Low Level		Sinking 1mA			0.4	V
EN3/SYNC						
EN3 Threshold High			2.4			V
EN3 Threshold Low					0.6	V
EN3 Internal Pulldown Resistance Value				500		kΩ
SYNC High-Switching Threshold			1.4			V
SYNC Low-Switching Threshold					0.4	V
SYNC Internal Pulldown Resistor Value				200		kΩ
INA POWER INPUT						
INA Input-Supply Range			3		5.5	V
INA Undervoltage-Lockout Threshold		V_{INA} rising, hysteresis = 200mV	2.5	2.7	2.9	V
INA Supply Current	I_{INA}	V_{FBP} = V_{FBGH} = 1.3V, V_{FBN} = V_{FBGL} = 0V, LXN and LXP not switching, VCOMH/L = OFF		0.6	3.0	mA
INA Supply Current, Shutdown Mode	I_{INA_SHDN}	V_{ENP} = 0V		1.2		µA
Duration-to-Trigger Fault Condition		V_{FBP}, V_{FBN}, V_{FBGH}, or V_{FBGL} below their PGOOD thresholds		218		ms
REFERENCE						
REF Output Voltage	V_{REF}	No load	1.238	1.25	1.262	V
REF Load Regulation		0 < I_{LOAD} < 80µA (load sink)	-0.6		+0.3	%
REF Undervoltage-Lockout Threshold		Rising edge, hysteresis = 200mV			1.15	V
OSCILLATOR						
Frequency	f_{OSC}		4320	4800	5280	kHz
Spread-Spectrum Modulation Frequency	f_{SS}			1200		kHz
Spread-Spectrum Factor	SSR	As a percentage of f_{OSC}		+8		%
BOOST AND CUK CONVERTERS—COMMON PARAMETERS						
Switching Frequency	f_{SW}			f_{OSC}/4		kHz
Switching Frequency Maximum Duty Cycle				93		%

Electrical Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LXP, LXN Current Limit	I_{LIM}	V_{VSH} = 16V, V_{VSL} = -12V, VSHLIM[1:0] = VSLLIM[1:0] = 00, default; see the *Applications Information* section for SPI programming of other values	1.3	1.56	1.87	A
LXP, LXN On-Resistance	R_{DS_ON}	$I_{LX\_}$ = 100mA		340	500	mΩ
LXP, LXN Leakage Current	I_{LEAK_LX}	$V_{LX\_}$ = 20V, T_A = +25°C		10	20	µA
Soft-Start Current		V_{VSH} = 16V, V_{VSL} = -12V, VSHLIM66 = VSLLIM66 = 0, default; see the *Applications Information* section for SPI programming of other values	1.3	1.56	1.87	A
Soft-Start Voltage Ramp Time				13.5		ms
FBP/FBN to COMPP/COMPN Transconductance		ΔI = ±2.5µA at COMPP/COMPN		400		µS
Internal Slope Compensation				1.5		A/µs
BOOST CONVERTER (VSH)						
Output Voltage Range	V_{VSH}		V_{INA}		18	V
FBP Regulation Voltage	V_{FBP}	V_{INA} = 3V to 5.5V	0.98	1	1.02	V
PGOOD Threshold	PGTSH	Measured on FBP		850		mV
FBP Load Regulation		0 < I_{LOAD} < full load		-1		%
FBP Line Regulation		V_{INA} = 3V to 5.5V		0.1		%/V
FBP Input-Bias Current		V_{FBP} = 1V, T_A = +25°C			1	µA
CUK CONVERTER (VSL)						
VSL Output Voltage Range	V_{VSL}	Using Cuk topology	-12		-4.5	V
FBN Regulation Voltage	V_{FBN}	Voltage that appears across feedback resistors connected between REF and FBN, V_{INA} = 3V to 5.5V	0.98	1	1.02	V
PGOOD Threshold	PGTSL	Measured on FBN, value referred to GND		400		mV
FBN Load Regulation				1		%
FBN Line Regulation		V_{INA} = 3V to 5.5V		0.3		%/V
FBN Input-Bias Current		V_{FBN} = 0.25V, T_A = +25°C			±1	µA
FBN Threshold Voltage for High-Power Boost Mode	V_{FBN}	LXN and LXP connected together for 2x output current capability		2.5		V
VGH LINEAR REGULATOR						
Output-Voltage Range	V_{VGH}	V_{VCP} = 23V, I_{LOAD} = 20mA	5		21	V
VGH Output Current	I_{VGH}	V_{VCP} - V_{VGH} = 2V	20			mA
FBGH Regulation Voltage	V_{FBGH}	I_{VGH} = 1mA	0.77 x V_{REF}	0.80 x V_{REF}	0.83 x V_{REF}	V
PGOOD Threshold	PGTGH	Measured on FBGH, V_{VGH} rising		850		mV

Electrical Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBGH Line Regulation		V_{VCP} = 12V to 20V at V_{VGH} = 10V, I_{VGH} = 10mA		2		%
FBGH Load Regulation		I_{VGH} = 0 to 20mA		2		%
FBGH Input-Bias Current		V_{FBGH} = 1V, T_A = +25°C			1	µA
VGH Current Limit	I_{LIMVGH}	T_A = +25°C	25	40		mA
VGH Soft-Start Time		VGHSTT[1:0] = 00, default		6.78		ms
		VGHSTT[1:0] = 10		13.6		
		VGHSTT[1:0] = 01		27.1		
		VGHSTT[1:0] = 11		54.3		
VGL LINEAR REGULATOR						
FBGL Regulation Voltage	V_{FBGL}	Voltage that appears across feedback resistors connected between REF and FBGL, I_{DRVN} = 100µA	0.77 x V_{REF}	0.8 x V_{REF}	0.83 x V_{REF}	V
Output Voltage Range	DRVN		-21		-2	V
FBGL PGOOD Threshold	PGTGL	Measured on FBGL, value referred to GND		400		mV
FBGL Input-Bias Current		V_{FBGL} = 0.25V, T_A= +25°C			±1	µA
DRVN Source Current		V_{FBGL} = 0.5V, V_{DRVN} = -10V	2			mA
DRVN Source Current Limit		T_A= +25°C	2.5	4		mA
VGL Soft-Start Time		VGLSTT[1:0] = 00, default		6.78		ms
		VGLSTT[1:0] = 10		13.6		
		VGLSTT[1:0] = 01		27.1		
		VGLSTT[1:0] = 11		54.3		
VCOMH BUFFER						
VCOMP Supply Range			6		18	V
VCOMP Supply Current		Buffer configuration, no load, no input, T_A = +25°C		3	5	mA
VCINH Resistive Divider Value		Internal 1MΩ pullup to VCOMP and 1MΩ pulldown to ground		500		kΩ
Input/Output Voltage Range			2		V_{VCOMP} - 2V	V
Large-Signal Voltage Gain		V_{VCOMH} = 2V to V_{VSH} - 2V		80		dB
Slew Rate		V_{VSH} = 12V, C_L < 30pF		45		V/µs
-3dB Bandwidth		V_{VSH} = 12V, C_L < 30pF		20		MHz
Current Limit		Sourcing, T_A = +25°C	90			mA
		Sinking, T_A = +25°C	90			
VCOML BUFFER						
VCOMN Supply Range			-7		-4.5	V
VCOMN Supply Current		Buffer configuration, no input, no load, T_A = +25°C		3	5	mA

Electrical Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCINL Resistance		Resistor internally connected to ground		1000		kΩ
Input Common-Mode Voltage Range		T_A = -40°C to +85°C	±1	±1.25		V
		T_A = +85°C to +105°C	±0.8			
Large-Signal Voltage Gain		V_{COML} = -1V to +1V		80		dB
Slew Rate		C_L < 30pF		28		V/µs
-3dB Bandwidth		C_L < 30pF		20		MHz
Current Limit		Sourcing	11			mA
		Sinking	11			mA
VCOM DAC						
Voltage Resolution				7		Bits
Differential Nonlinearity		Monotonic over temperature (Note 5)	-1		+1	LSB
Zero-Scale Error		Includes V_{COMH} or V_{COML} buffer input offset voltage	-2		+2	LSB
Full-Scale Error			-12		+12	LSB
VCOM Voltage Step Size				7.8		mV
INPUT AND OUTPUT SERIES SWITCH CONTROL						
p-Channel FET Gate-Driver Sink Current		V_{GATE} = V_{INA}	36	53	70	µA
p-Channel Gate-Driver Voltage Threshold		Measured at GATE; below this voltage, the external p-channel FET is conducting		1.25		V
VSLS Gate-Driver Source Current		V_{VSLS} = -5V	38	50	58	µA
DIGITAL INPUTS						
$\overline{CS}$ Input Pullup Resistor Value	R_{PU}			500		kΩ
SSEN, ENP Input Pulldown Resistor Value	R_{PD}			500		kΩ
ENP, EN1, EN2, CLK, $\overline{CS}$, DIN, SSEN Input Voltage Low	V_{IL}				0.8	V
ENP, EN1, EN2, CLK, $\overline{CS}$, DIN, SSEN Input Voltage High	V_{IH}		2.4			V
DIGITAL OUTPUTS						
DOUT Output Voltage Low					0.4	V
DOUT Output Voltage High			2.8			V
$\overline{FLT}$ Output Voltage Low	$V_{\overline{FLT}}$	I_{SINK} = 2mA			0.4	V
SPI INTERFACE (Note 6)						
Clock Frequency	f_{CLK}				4	MHz
Falling Edge of $\overline{CS}$ to Rising Edge of CLK Required Setup Time	t_{LEAD}	Input rise/fall time < 10ns	100			ns
Falling Edge of CLK to Rising Edge of $\overline{CS}$ Required Hold Time	t_{LAG}	Input rise/fall time < 10ns	100			ns

Electrical Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time DIN-to-CLK Falling Edge	$t_{DIN(SU)}$		30			ns
DIN Hold Time after Falling Edge of CLK	$t_{DIN(HOLD)}$		20			ns
Time from Rising Edge of CLK-to-DOUT Data Valid	t_{VALID}	C_{DOUT} = 50pF			70	ns
Time from Falling Edge of $\overline{CS}$ to DOUT Low	$t_{DOUT(EN)}$				55	ns
Time from Rising Edge of $\overline{CS}$ to DOUT High Impedance	$t_{DOUT(DIS)}$				55	ns
DOUT Leakage Current in High-Impedance State	$I_{DOUT(HI-Z)}$	$V_{\overline{CS}}$ = V_{INA}, V_{DOUT} = V_{INA}/2, T_A = +25°C			1	µA
$\overline{FLT}$ Leakage Current in High-Impedance State	$I_{\overline{FLT}(HI-Z)}$	$V_{\overline{FLT}}$ = 5V, T_A = +25°C			1	µA
EN1/EN2/CLK Leakage Current	I_{IN_LEAK}	3.3V < V_{INA} ≤ 5.0V, T_A = +25°C			1	µA
DIN Input Pulldown Resistor Value	$R_{PD,DIN}$			50		kΩ
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				15		°C

Note 3: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 4: Guaranteed by design; not production tested.
Note 5: Design guaranteed by ATE characterization. Limits are not production tested.
Note 6: Guaranteed by design. Figure 1 shows the SPI timing characteristics.

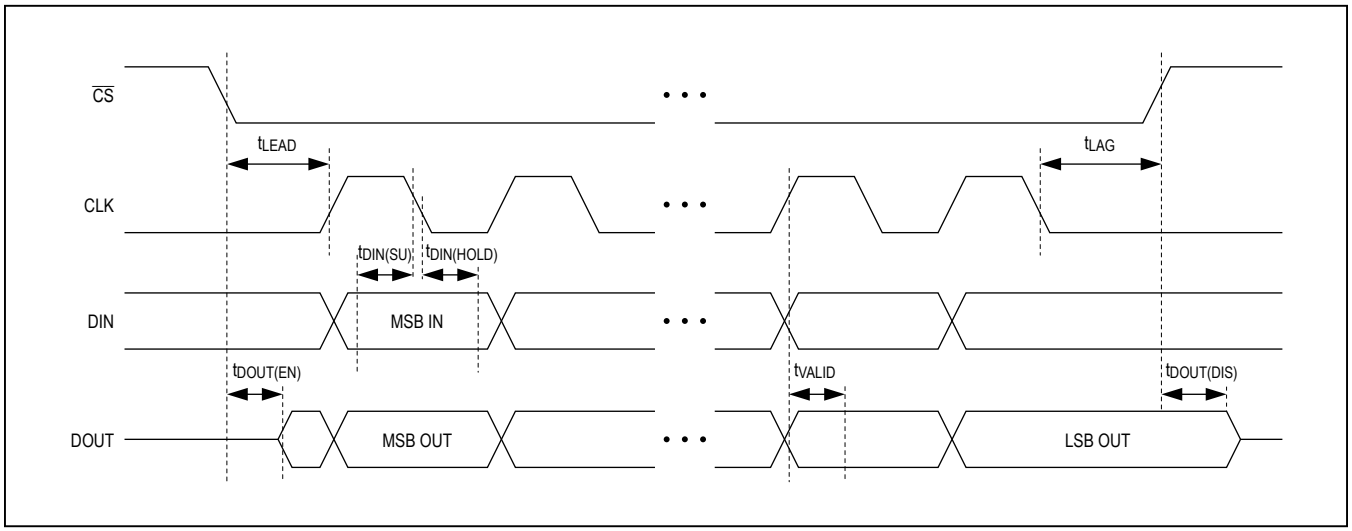
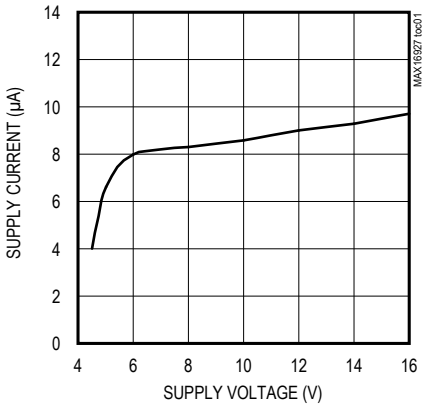


Figure 1. SPI Timing Characteristics

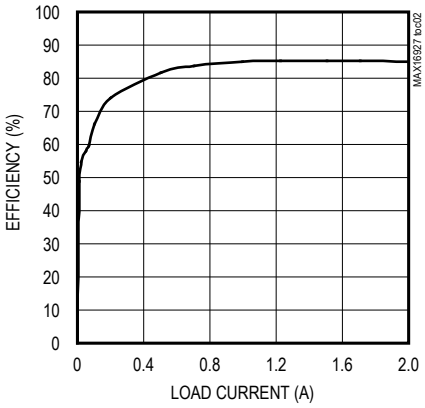
Typical Operating Characteristics

(V_{IN3} = 12V, V_{INA} = 3.3V, V_{VGH} = 12V, V_{VGL} = -12V, V_{VSH} = 6.9V, V_{VSL} = -6.9V, T_A = +25°C, unless otherwise noted.)

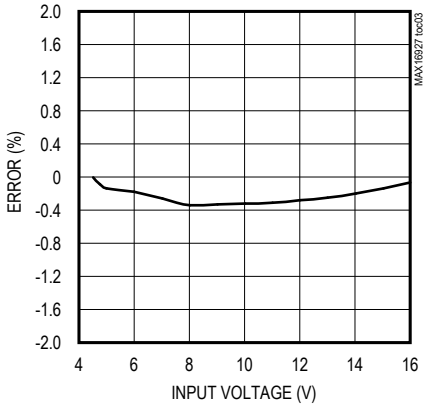
SHUTDOWN SUPPLY CURRENT (BUCK)



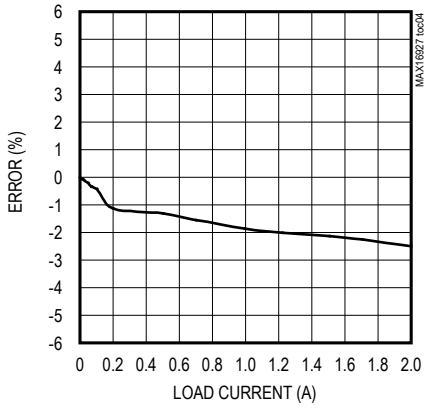
EFFICIENCY vs. LOAD CURRENT (BUCK)



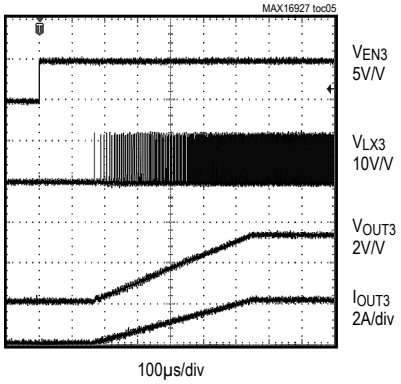
LINE REGULATION (BUCK)



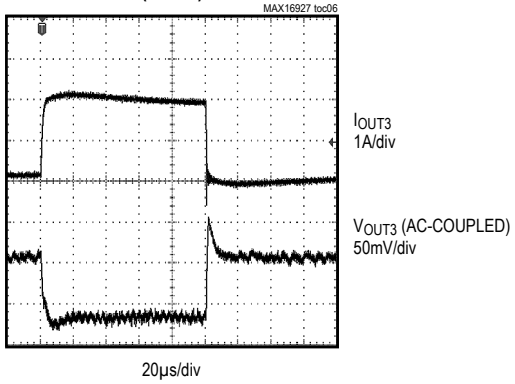
LOAD REGULATION (BUCK)



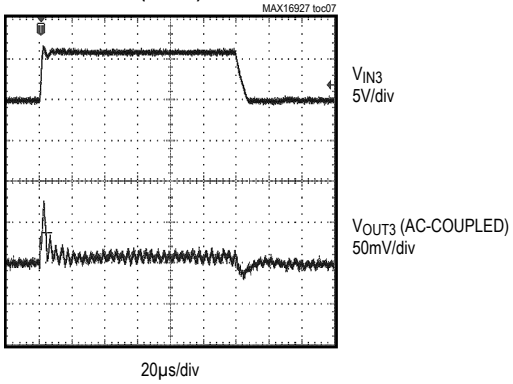
STARTUP BEHAVIOR (BUCK)



100mA TO 2A LOAD TRANSIENT RESPONSE (BUCK)



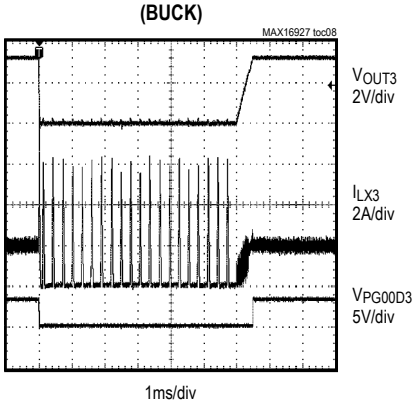
10V TO 16V LINE TRANSIENT RESPONSE (BUCK)



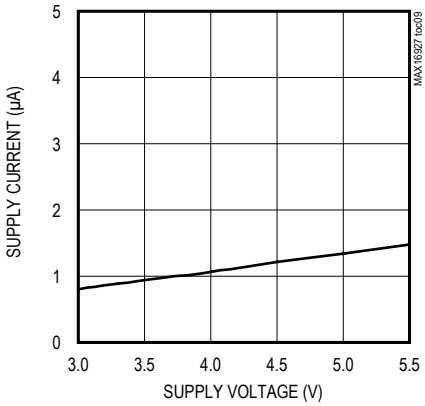
Typical Operating Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, V_{VGH} = 12V, V_{VGL} = -12V, V_{VSH} = 6.9V, V_{VSL} = -6.9V, T_A = +25°C, unless otherwise noted.)

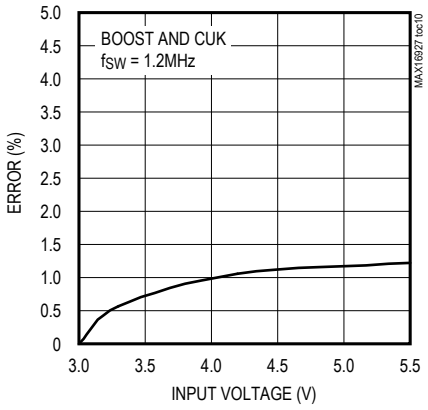
SHORT-CIRCUIT BEHAVIOR (BUCK)



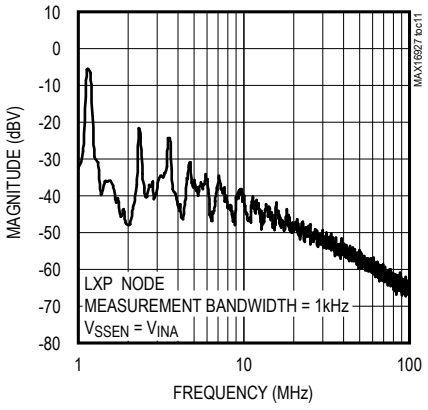
INA SHUTDOWN SUPPLY CURRENT



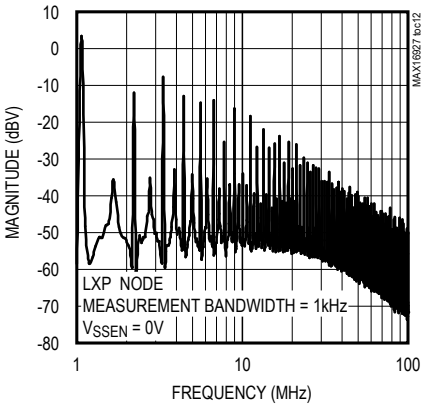
SWITCHING FREQUENCY vs. SUPPLY VOLTAGE



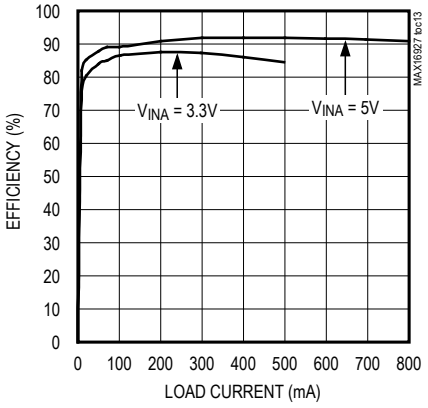
SPECTRUM (SPREAD-SPECTRUM MODE)



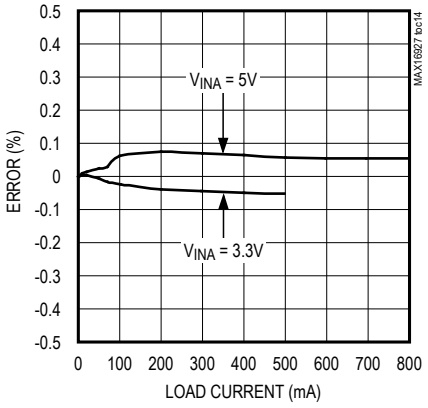
SPECTRUM (FIXED-FREQUENCY MODE)



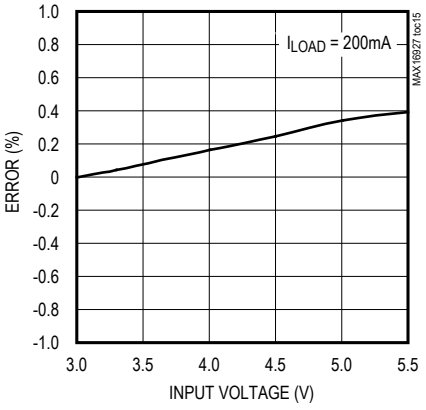
EFFICIENCY vs. LOAD CURRENT (BOOST)



LOAD REGULATION (BOOST)



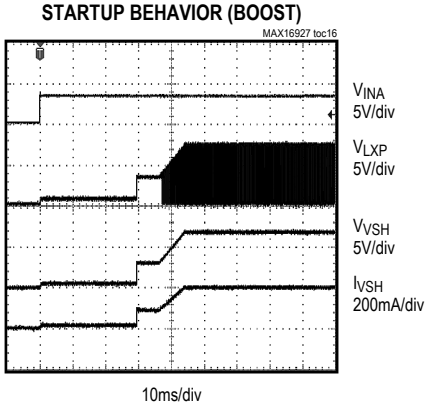
LINE REGULATION (BOOST)



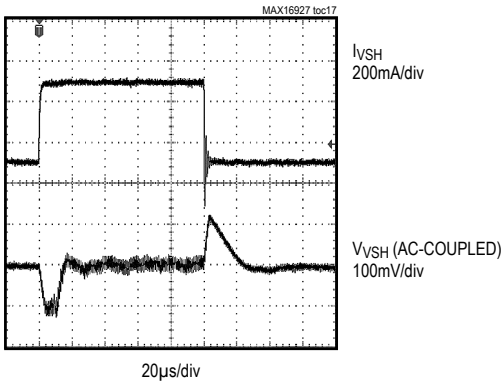
Typical Operating Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, V_{VGH} = 12V, V_{VGL} = -12V, V_{VSH} = 6.9V, V_{VSL} = -6.9V, T_A = +25°C, unless otherwise noted.)

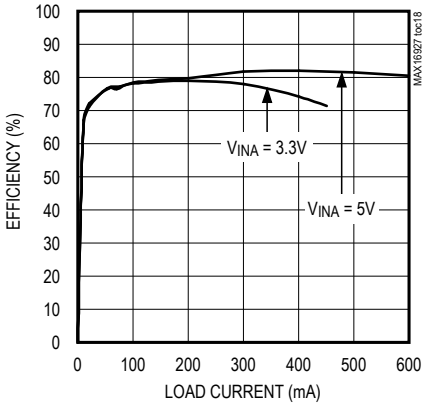
STARTUP BEHAVIOR (BOOST)



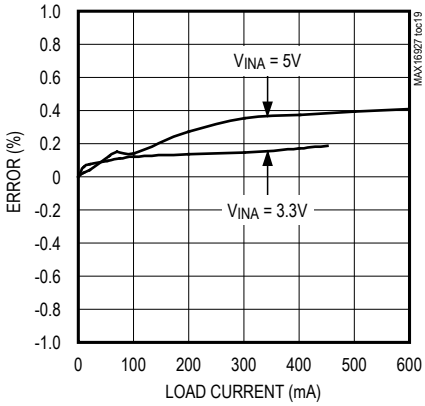
100mA TO 500mA LOAD TRANSIENT RESPONSE



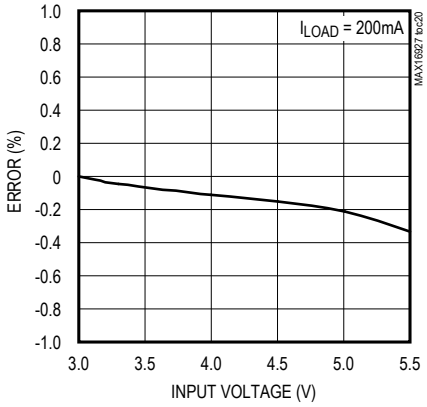
EFFICIENCY vs. LOAD CURRENT (CUK)



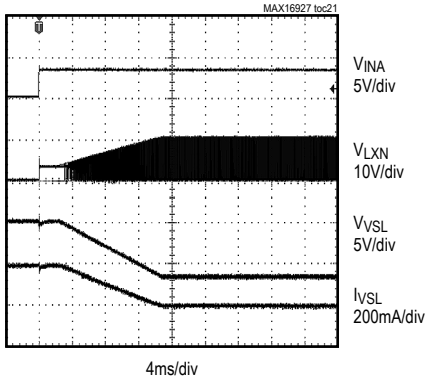
LOAD REGULATION (CUK)



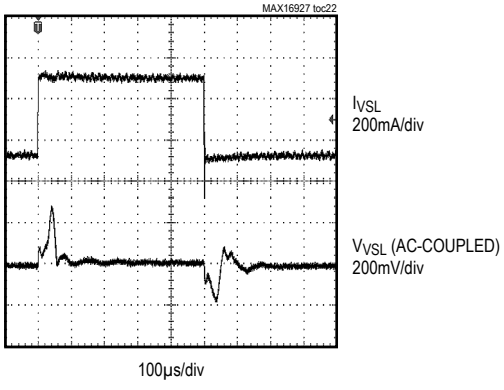
LINE REGULATION (CUK)



STARTUP BEHAVIOR (CUK)



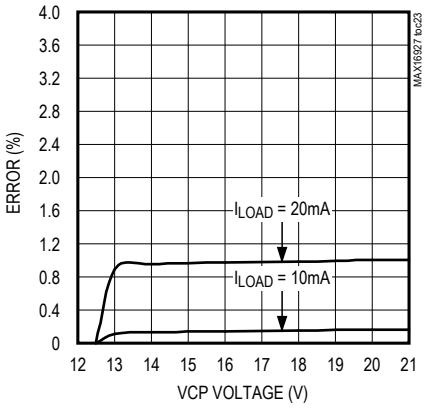
100mA TO 450mA LOAD TRANSIENT RESPONSE



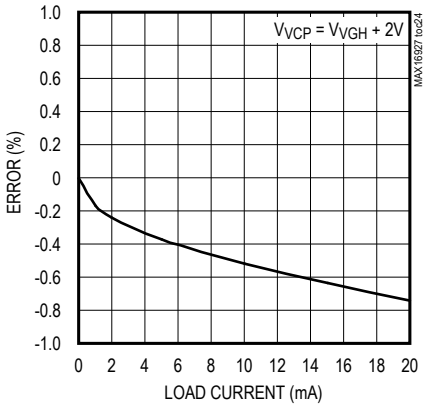
Typical Operating Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, V_{VGH} = 12V, V_{VGL} = -12V, V_{VSH} = 6.9V, V_{VSL} = -6.9V, T_A = +25°C, unless otherwise noted.)

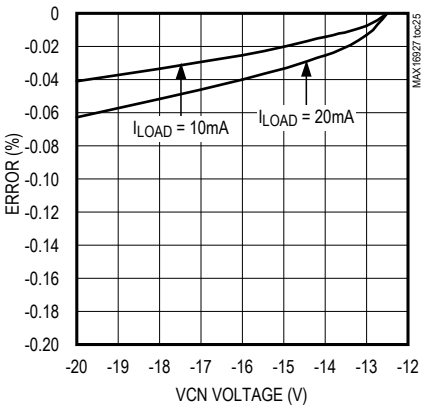
LINE REGULATION (VGH LINEAR REGULATOR)



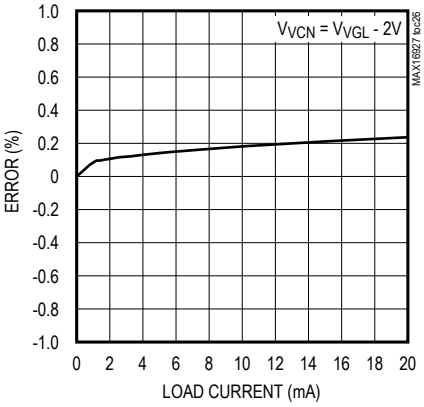
LOAD REGULATION (VGH LINEAR REGULATOR)



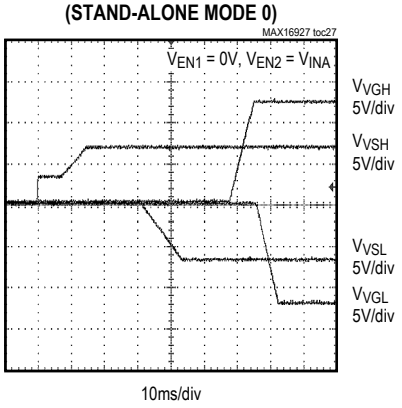
LINE REGULATION (VGL LINEAR REGULATOR)



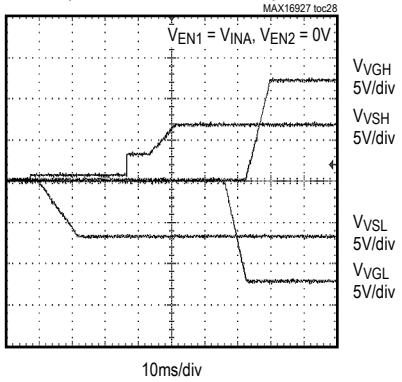
LOAD REGULATION (VGL LINEAR REGULATOR)



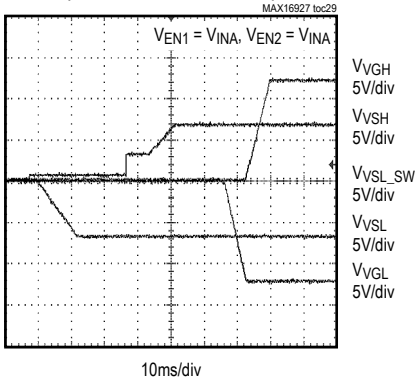
SUPPLY SEQUENCING (STAND-ALONE MODE 0)



SUPPLY SEQUENCING (STAND-ALONE MODE 1)



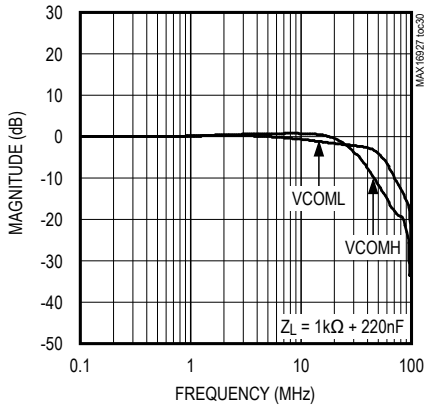
SUPPLY SEQUENCING (STAND-ALONE MODE 2)



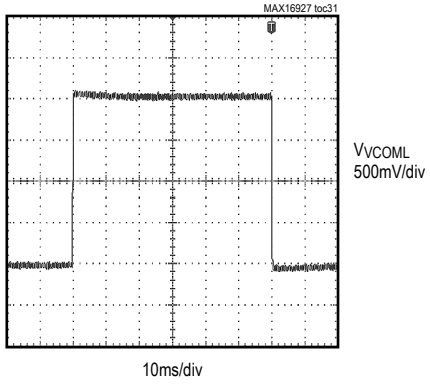
Typical Operating Characteristics (continued)

(V_{IN3} = 12V, V_{INA} = 3.3V, V_{VGH} = 12V, V_{VGL} = -12V, V_{VSH} = 6.9V, V_{VSL} = -6.9V, T_A = +25°C, unless otherwise noted.)

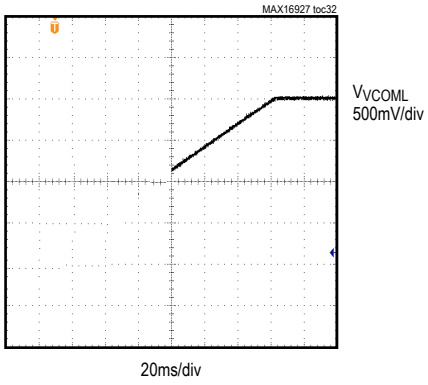
MAGNITUDE RESPONSE vs. FREQUENCY (VCOM BUFFER)



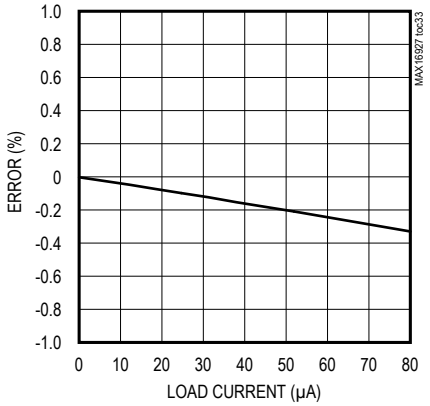
VCOML TRANSIENT RESPONSE



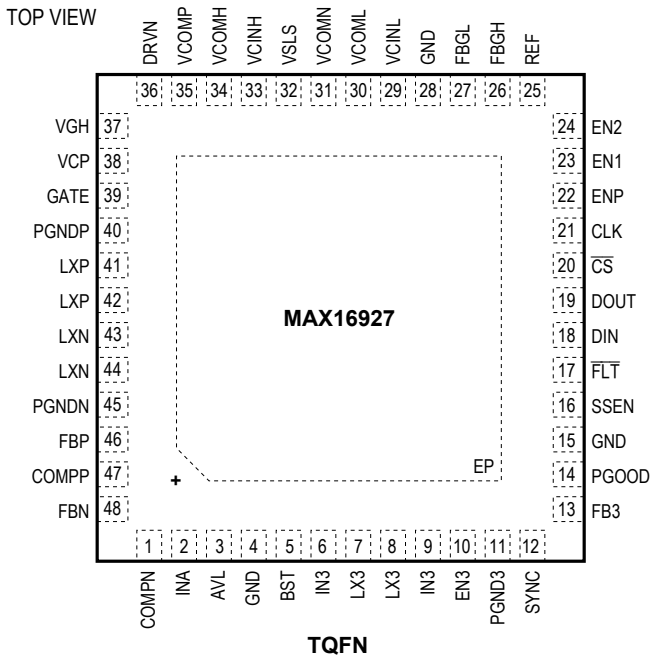
RAMPED DAC RESPONSE



REFERENCE LOAD REGULATION



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	COMPN	Cuk Converter Error-Amplifier Compensation. Connect the compensation network from COMPN to GND.
2	INA	Boost and Cuk Power Supply. Connect to the output of the buck converter or to a supply between 3V and 5.5V.
3	AVL	Buck Converter Internal 5V Regulator. Connect a 1µF capacitor between AVL and PGND3. Do not use AVL to power external circuitry.
4, 15, 28	GND	Analog Ground
5	BST	Buck Converter Bootstrap Capacitor Connection. Connect a 0.1µF capacitor between BST and LX3.
6, 9	IN3	Buck Converter Power Supply. Connect to a 4.5V to 16V supply. Connect a 1µF or larger ceramic capacitor in parallel with a 47µF capacitor from IN3 to PGND3. Connect both IN3 power inputs together.
7, 8	LX3	Buck Converter Inductor Connection. Connect the inductor, boost capacitor, and catch diode at this node.
10	EN3	Buck Converter Enable Input. EN3 is a high-voltage, 5V- and 3.3V-compatible input. Connect to IN3 for normal operation and connect to PGND3 to disable the buck converter.
11	PGND3	Buck Converter Power Ground
12	SYNC	Buck Converter Sync Input. SYNC allows the buck converter to be synchronized to other DC-DC converters. When connected to an external clock source, the buck converter is synchronized. When SYNC is not used, connect to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
13	FB3	Buck Converter Feedback Input. Connect FB3 to the output-voltage node, OUT3, as shown in the *Typical Operating Circuits*.
14	PGOOD	Buck Converter Open-Drain Power-Good Output. Connect a 10kΩ pullup resistor to any low-voltage supply.
16	SSEN	Spread-Spectrum Enable Input. Connect SSEN to INA to place the boost and Cuk in spread-spectrum mode. Connect SSEN to GND for fixed-frequency PWM operation. SSEN has an internal 500kΩ pulldown resistor.
17	$\overline{FLT}$	Open-Drain Fault Output. When low, $\overline{FLT}$ indicates that one or more of the output voltages (except the buck-converter output) are less than 85% of their regulated values. Connect a 10kΩ pullup resistor from $\overline{FLT}$ to INA. The $\overline{FLT}$ output is cleared on the rising edge of the $\overline{CS}$ signal or when ENP is toggled.
18	DIN	SPI Interface Data Input. Data is clocked in on the falling edge of the CLK input. DIN has an internal 50mΩ (typ) pulldown resistor.
19	DOUT	SPI Interface Data Output. Data is stable on the falling edge of the CLK input.
20	$\overline{CS}$	SPI Interface Active-Low Chip-Select Input. Pull $\overline{CS}$ low to enable the SPI interface. A new 32-bit data word is latched into the input register on the rising edge of $\overline{CS}$. When $\overline{CS}$ is high, DOUT is high impedance. $\overline{CS}$ has an internal pullup resistor of value of 500kΩ.
21	CLK	SPI Interface Clock Input
22	ENP	Active-High Enable Input. ENP enables the device, with the exception of the buck converter, which is controlled by EN3. ENP has an internal 500kΩ pulldown resistor. To enable the boost converter, take ENP high when INA > 2.9V. Connect ENP to GND to place everything in shutdown except the buck converter.
23	EN1	Enable Input 1. EN1 and EN2 determine the supply sequencing of the regulators. When EN1 and EN2 are low, the SPI interface is enabled. See the ***Soft-Start and Supply Sequencing (EN3, ENP, EN1, EN2)*** section.
24	EN2	Enable Input 2
25	REF	1.25V Reference Output. Connect a 100nF capacitor between REF and GND.
26	FBGH	Positive Gate-Voltage Linear Regulator-Feedback Input. FBGH is regulated to 1V.
27	FBGL	Negative Gate-Voltage Linear Regulator-Controller-Feedback Input. FBGL is regulated to 0.25V.
29	VCINL	VCOML Adder Input. The voltage on VCINL is added to the VCOM DAC voltage and buffered to the VCOML output.
30	VCOML	Low-Range VCOM Buffer Output. The output range of this buffer can be DAC from 0V to 1V around the VCINL voltage.
31	VCOMN	VCOML Buffer Negative Supply. The positive supply for this buffer is INA. If V_{VSL} is set lower than -7V, an external regulator is needed to limit V_{VCOMN} to -7V.
32	VSLS	External n-Channel FET Gate Drive. VSLS sources a current to turn on the external FET when the ENVSLS bit is set to 1 through SPI.
33	VCINH	VCOMH Adder Input. The voltage on VCINH is added to the VCOM DAC voltage and buffered to the VCOMH output.
34	VCOMH	High-Range VCOM Buffer Output. The output range of this buffer can be DAC from 0V to 1V around the VCINH voltage.
35	VCOMP	VCOMH Buffer Positive Supply. The negative supply for this buffer is GND. Connect VCOMP to the output of the boost converter even if the VCOMH buffer is unused.

Pin Description (continued)

PIN	NAME	FUNCTION
36	DRVN	Negative Gate-Voltage Linear Regulator Base Drive Output. Open drain of an internal n-channel FET. Connect DRVN to the base of an external npn pass transistor.
37	VGH	Positive Gate-Voltage Linear Regulator Output
38	VCP	Positive Gate-Voltage Linear Regulator Power Input. Connect VCP to the positive output of the external charge pump.
39	GATE	External p-Channel FET Gate Drive. GATE sinks a current to turn on the external FET when the boost converter is enabled and goes into high impedance during a fault condition or when the boost is disabled.
40	PGNDP	Boost Converter Power Ground
41, 42	LXP	Boost Converter Switching Node. Connect the inductor and diode to this node.
43, 44	LXN	Cuk Converter Switching Node. Connect the inductor and coupling capacitor to this node.
45	PGNDN	Cuk Converter Power Ground
46	FBP	Boost Converter Feedback Input. FBP is regulated to 1V.
47	COMPP	Boost Converter Error-Amplifier Compensation. Connect the compensation network from COMPP to GND.
48	FBN	Cuk Converter Feedback Input. FBN is regulated to 0.25V. Connect FBN to INA when LXN and LXP are connected together to double the output power of the boost.
—	EP	Exposed Pad. Connect the exposed pad to the ground plane for optimal heat dissipation. Do not use the exposed pad as the only electrical ground connection.

Detailed Description

The MAX16927 is a highly integrated power supply for automotive TFT-LCD applications. The device integrates one buck converter to generate 3.3V from a 4.5V to 16V supply, one boost converter, one Cuk converter, two gate-voltage controllers, and two VCOM buffers, one of which supports an active ±1V drive referred to GND. An SPI interface provides diagnostics and host control.

The buck converter operates independently from the boost and Cuk converters and the linear regulators. Use the buck converter to generate a 3.3V output to power the other four regulators from a 4.5V to 16V supply. Alternatively, power the four regulators from an available 3V to 5.5V supply and ground all pins for the buck converter: BST, IN3, LX3, FB3, EN3, AVL, PGOOD, SYNC, and PGND3.

3.3V Buck Converter

The device features a current-mode buck converter with an integrated high-side FET, which requires no external compensation network. The device regulates the output voltage to 3.3V. The buck converter delivers a minimum of 2A of output current. The high 2.1MHz (typ) switching frequency allows for small external components, reduced output ripple, and guarantees no AM interference.

A power-good (PGOOD) indicator is available to monitor output-voltage quality. Shutting down the buck converter reduces the supply current to 10µA.

Enable (EN3)

The buck converter is activated by driving EN3 high. EN3 is compatible with +3.3V logic levels but is also high-voltage compatible up to 20V. The EN3 input has a 500kΩ pulldown resistor.

Undervoltage Lockout (UVLO)

When the device is enabled, an internal bias generator turns on. LX begins switching after V_{AVL} has exceeded the internal UVLO level V_{UVLO} = 2.7V (typ).

Soft-Start

The buck converter goes into soft-start after four current-limit events have been detected. Upon detecting the fourth current-limit event, the device starts the soft-start timer and attempts to ramp the output to its final value in 1024 clock cycles (t_{SS} = 0.49ms typ). If the output does not reach its final value before the soft-start timer expires, the buck converter stops switching for 576 clock cycles before reattempting to regulate the output. The process repeats until the source of output undervoltage is removed.

Oscillator/Synchronization (SYNC)

The buck converter has an integrated oscillator that provides a switching frequency of 2.1MHz (typ). The SYNC pin can be used to synchronize the internal clock with an external source. Use an external clock frequency range between 1.8MHz and 2.6MHz. Connect SYNC to GND if not used.

Spread-Spectrum Mode

The buck converter features spread-spectrum operation, which varies the internal operating frequency of the buck converter by +6% relative to the internally generated operating frequency of 2.1MHz (typ). This function does not apply to an externally applied clock signal.

Power-Good (PGOOD)

The buck converter features an open-drain power-good output. PGOOD is an active-high output that pulls low when the buck output voltage is below 90% of its nominal value and is high impedance when the output voltage is above 92% of its nominal value. Connect a 10kΩ pullup resistor from PGOOD to any low-voltage supply.

Overcurrent Protection

The buck converter limits its output current to I_{MAX} = 2.72A (min). If a short-circuit condition is detected for four clock cycles, the controller stops switching for 512 clock cycles and attempts to soft-start the output. This process is repeated until the short-circuit condition is removed. In the event the internal FET overheats, the device enters thermal-overload protection.

Internal 5V Regulator (AVL)

The device features a 5V regulator whose function is to charge the boost capacitor through the internal boost diode and to power the circuitry of the buck converter. Bypass AVL to GND with a 1µF capacitor. Do not use AVL to power external circuitry.

Oscillator and Spread-Spectrum Mode (Boost and Cuk)

The boost and Cuk converters run from a 1.2MHz oscillator. Connect SSEN to INA to enable spread-spectrum clocking, in which the clock frequency varies +8% above 1.2MHz. Connect SSEN to GND for fixed-frequency 1.2MHz clocking.

Boost Converter

The boost converter employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads typical of TFT-LCD panel source drivers. The 1.2MHz switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start functions reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{INA} to 18V with an external resistive voltage-divider. The regulator controls the output voltage by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D = \frac{V_{VSH} - V_{INA}}{V_{VSH}}$$

Figure 2 shows the functional diagram of the boost regulator. An error amplifier compares the signal at FBP to 1V and changes the COMPP output. The voltage at COMPP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMPP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal. On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum

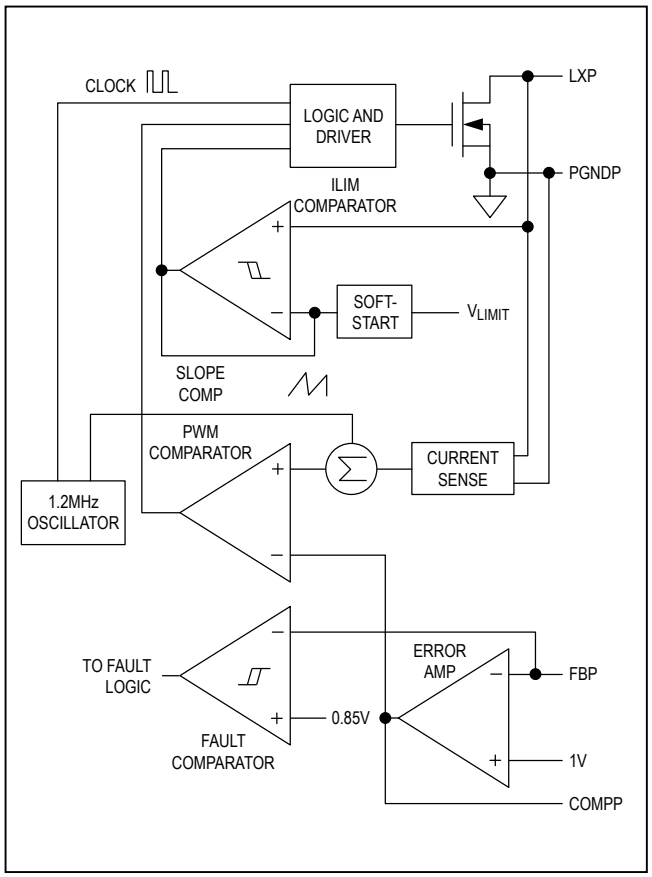


Figure 2. Boost Converter Functional Diagram

of the current-feedback signal and the slope compensation exceeds the COMPP voltage, the controller resets the flip-flop and turns off the MOSFET. The inductor current then flows through the diode to the output. The MOSFET remains off for the rest of the clock cycle.

The external p-channel FET controlled by GATE protects the output during fault conditions and makes possible true shutdown of the converter. During startup, VSH is slightly prebiased to detect any shorts on the boost output. Under normal operation, the p-channel FET is turned on, connecting the supply to the input of the boost converter. Under a fault condition or in shutdown, the FET is turned off, disconnecting the supply from the input and preventing current from charging the output through the inductor and diode from the supply.

Cuk Converter

The Cuk converter produces a negative output using a controller architecture similar to that of the boost. The network—LN1, C1, and Schottky diode—allow a boosted voltage to be stored on C1 (see Figure 3). Ignoring parasitic voltage drops, the relationship between V_{C1} and V_{INA} is given by:

$$\frac{V_{C1}}{V_{INA}} = \frac{1}{1-D}$$

During the on-time, energy is stored in LN1 and during the off-time it is released to storage capacitor C1. The network—C1, Schottky diode, LN2, and C2—performs the inverting function. Ignoring parasitic voltage drops, the relationship between the output of the Cuk converter and V_{C1} is given by:

$$\frac{V_{VSL}}{V_{C1}} = -D$$

During the on-time, C1 delivers energy to C2, the load, and LN1. During the off-time, LN1 releases the energy stored during the on-time to C2 and the load. The relationship between input and output voltages is:

$$\frac{V_{VSL}}{V_{INA}} = -\frac{D}{1-D}$$

During startup, depending on the configuration of EN1 and EN2, the n-channel FET gating the Cuk output is turned off to allow the charge-pump voltages to settle to their final values. The charge pumps power the positive and negative gate-voltage regulators, VGH and VGL. Turn on the n-channel FET and connect the Cuk output to VSL by setting the EN_VSLS bit to 1.

When VCOMN is connected to the output of the Cuk converter, V_{VSL} must be limited to -7V. If V_{VSL} is set lower than -7V, an external regulator is needed to limit the voltage on VCOMN to -7V.

High-Power Boost Converter

Figure 10 shows an alternative use of the Cuk converter power stage. Disabling the Cuk by connecting FBN to INA and using the boost and Cuk power stages in parallel provides a boost converter output capable of twice the power by doubling the inductor current limit. In this application, connect LXN and LXP together and leave VSLS unconnected.

Current Limit (Boost and Cuk)

The effective current limit is reduced by the internally injected slope compensation by an amount dependent on the duty cycle of the converter. The effective current limit is given by:

$$I_{LIM(EFF)} = I_{LIM\_DC\_0\%} - 1.16 \times \frac{D}{93\%}$$

for $I_{LIM\_DC\_0\%}$, dependence on SPI bits VSxLIM<66,1,0> (Table 1). The VSxLIM[66] bit determines whether during soft-start the current limit is reduced one level down. After soft-start is finished, the VSxLIM[66] bit has no influence. The Cuk converter exhibits a similar reduction in current limit dependent on its duty cycle. With the Cuk converter current limit bits set to 0 (i.e., VSLLIM1 = VSLLIM0 = 0), the effective current limit is given by the same equation where D is the duty cycle of the Cuk converter in percent. Estimate the duty cycle of each converter using the formulas shown in the ***Design Procedure*** section. Figure 4 shows the dependence of the current limit on the duty cycle of the boost and Cuk converters.

EMI Reduction

The device reduces the EMI of the boost and Cuk converters in two ways. In spread-spectrum mode, the switching frequency of the boost and Cuk converters varies randomly to +8% of 1.2MHz.

Additional EMI reduction is achieved by running the boost and Cuk converters 180 degrees out of phase. In a high-power boost converter as described in the previous section, the boost and Cuk converters run in phase. Table 2 summarizes the phase relationship between the boost and Cuk converters.

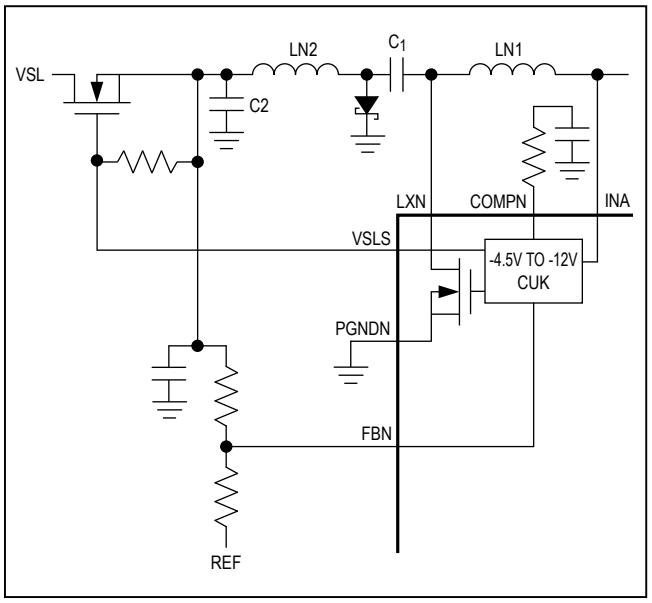


Figure 3. Cuk Converter

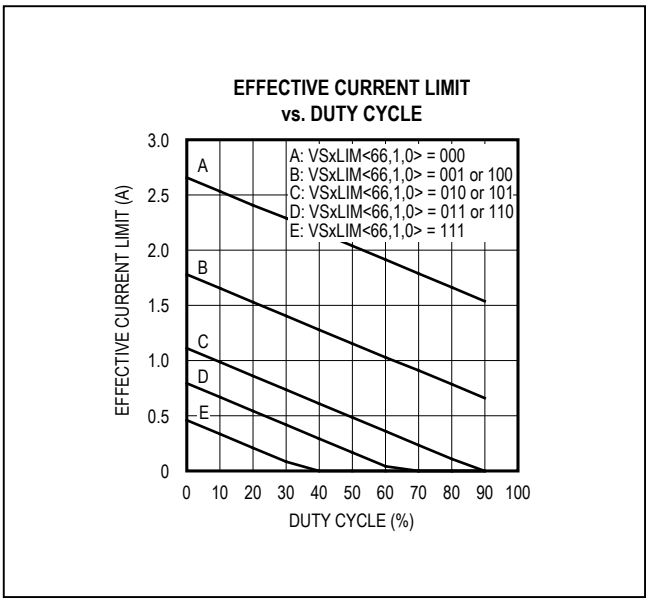


Figure 4. Effective Current Limit vs. Duty Cycle

Table 1. Boost and Cuk Current Limit Settings

SPI BITS VSxLIM<66,1,0>	$I_{LIM\_DC\_0\%}$ (A)
000	2.66
001 or 100	1.78
010 or 101	1.11
011 or 110	0.79
111	0.46

Note: *Codes with bit <66> high are applicable in soft-start only.*

Table 2. Phase Relationship Between Converters

APPLICATION	PHASE RELATIONSHIP BETWEEN BOOST AND CUK CONVERTERS
One positive output, one negative output	180 degrees out of phase
One higher power positive output	In phase

Positive Gate-Voltage Linear Regulator (VGH)

The positive gate-voltage linear-regulator includes a p-channel FET output stage to generate a regulated +5V to +22V output. The regulator maintains accuracy over wide line and load conditions. It is capable of at least 20mA of output current and includes current-limit protection. VGH is typically used to provide the TFT LCD gate drivers' gate-on voltage.

The VGH linear regulator derives its positive supply voltage from a noninverting charge pump, a single-stage example of which is shown in the *Typical Operating Circuits* (Figure 9 and Figure 10). A higher voltage using a multistage charge pump is possible as described in the ***Charge Pumps*** section.

Negative Gate-Voltage Linear-Regulator Controller (VGL)

The negative gate-voltage linear-regulator controller is an analog gain block with an open-drain p-channel output. It drives an external npn pass transistor with a 6.8kΩ base-to-emitter resistor (see the ***Pass Transistor Selection*** section). Its guaranteed base drive-source current is at least 2mA. VGL is typically used to provide the TFT LCD gate-drivers' gate-off voltage.

The VGL linear regulator derives its negative supply voltage from an inverting charge pump, a single-stage example of which is shown in the *Typical Operating Circuits*. A more negative voltage using a multistage charge pump is possible as described in the ***Charge Pumps*** section.

VCOM Buffers

The VCOM buffers, VCOMH and VCOML, hold their output voltage stable while providing the ability to source and sink a high current quickly into a capacitive load such as the backplane of a TFT LCD panel.

In stand-alone mode, the SPI interface is not used. The VCOMH and VCOML output voltages are set by applying voltages to the VCINH and VCINL inputs. VCINH is internally biased to midrail ($V_{VCOMP/2}$) using internal 1MΩ pullup and pulldown resistors. VCINL is internally pulled to ground through a 1MΩ resistor. Its voltage is adjustable using a single external resistor typically connected to VCOMN. Alternatively, to avoid drift in the voltage due to the difference in thermal coefficients between the internal and external resistors, set the voltage on VCINL using two lower value external resistors.

Only one VCOM buffer is active at a time. The VCOML buffer is active only when the Cuk converter is running while the VCOMH buffer is active only when the Cuk converter is disabled or paralleled with the boost converter to provide a high-power boosted output (i.e., FBN is connected to INA). Always connect VCOMP to the output of the boost converter, even when the VCOMH buffer is inactive.

The MAX16927 features a +7-bit VCOM digital-to-analog converter (DAC) whose output polarity and magnitude is controlled through SPI (see the ***VCOM DAC*** section). The resolution of the DAC is 7.8mV for a 0V to +1V output range. The output of the DAC is buffered to the VCOMH and VCOML outputs. Further offset is possible by applying a voltage to VCINH or VCINL. The VCOMH buffer is powered between VCOMP and GND while the VCOML buffer is powered between INA and VCOMN. Always connect VCOMP to the output of the boost converter even when the VCOMH buffer is inactive. Ensure that the voltage on VCOMN never falls below -7V.

Driving Purely Capacitive Loads

In general, the LCD backplane (VCOM) consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a purely capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω resistor placed between the buffer output and the capacitive load reduces peaking but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

Soft-Start and Supply Sequencing (EN3, ENP, EN1, EN2)

The device provides flexible supply-sequencing schemes. The order in which the switching and linear regulators turn on is determined either by the external enable inputs (ENP, EN3, EN1, and EN2) or through SPI. Table 3 shows the various supply-sequencing options available on the device. Do not connect ENP directly to INA; ENP should not transition from low to high until INA > 2.9V.

When enabled, the regulator ramps the output voltage toward its set voltage. The soft-start period of the boost and Cuk converters is a fixed 13.56ms. The soft-start period of the linear regulators is SPI controlled and is 6.784ms by default. Each regulator turns on immediately after the previous regulator's internal PGOOD indicator signals that its output is within regulation (i.e., within 85% of its set voltage). For the boost and Cuk converters after

Table 3. Supply Sequencing

ENABLE INPUT				SUPPLY-SEQUENCING ORDER				
EN3	ENP	EN1	EN2	1st	2nd	3rd	4th	5th
0	0	X	X	Device is in shutdown.				
1	0	X	X	Buck converter is outputting 3.3V. All other blocks are in shutdown.				
0	1	X	X	Buck converter is in shutdown. An external 3.3V to 5V supply powers INA.				
X	1	0	0	SPI determines which regulator is on.				
X	1	0	1	VSL	VSH	VGL	VGH	—
X	1	1	0	VSH	VSL	VGH	VGL	—
x	1	1	1	VSL	VGL	VSH	VGH	VSL switch

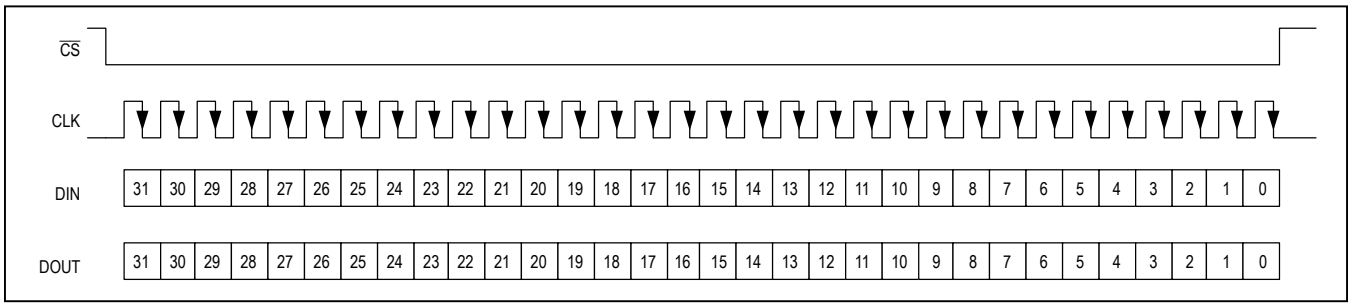


Figure 5. SPI Timing Diagram (CPOL = 0, CPHA = 1)

the ramp-up time of 13.56ms, there is a further 13.56ms delay before other regulators are enabled.

Fault Indicator ($\overline{FLT}$)

The active-low fault indicator pulls low when any of the switching or linear regulator output voltages (except for the buck converter) are out of regulation. An internal voltage monitor is available for each regulator. When the output voltage falls and stays below 85% of the set voltage for a duration of 218ms, $\overline{FLT}$ asserts. The fault-blanking time of 218ms prevents false triggering. There are PGOOD indicators for each regulator than can be read out through SPI so that the fault can be traced back to the failing supply.

An overvoltage condition on either LXN, LXP, the Cuk output, or the boost output causes $\overline{FLT}$ to assert immediately and the device to shut down. Once this fault condition is cleared, toggle ENP low for 1ms and then high to return the device to reinitiate the startup sequence. The device turns on the switching and linear regulators in the order shown in Table 3.

In the event of a thermal fault (i.e., the junction temperature T_J exceeds +165°C), $\overline{FLT}$ asserts immediately and the device shuts down. Once the device cools by 15°C, the device turns on the switching and linear regulators in the order shown in Table 3.

SPI-Compatible Serial Interface

The device has an SPI interface consisting of three inputs and one output: the clock signal (CLK), data input (DIN), chip-select input ($\overline{CS}$), and data output (DOUT). Use a clock frequency of 4MHz or less to communicate with the device. The serial interface works with the clock polarity (CPOL) set to 0 and the clock phase (CPHA) set to 1 (Figure 5). The device may also be used without the SPI interface (see the ***Stand-Alone Mode*** section).

Initiate a write to the device by pulling $\overline{CS}$ low and setting the MSB bit to 0. Data is written MSB first and is clocked in on the falling edge of each clock pulse. Each write to the device consists of 32 bits (1 word). Pull $\overline{CS}$ high after the 32nd bit has been clocked in to latch the data. The internal register is not updated if $\overline{CS}$ is pulled high before the falling edge of the 32nd clock pulse. The SPI interface only accepts data inputs of 32 bits or a multiple of 32 bits.

To read from the SPI register, write a word to the SPI interface with the MSB bit set to 1. The 31 remaining bits are don't cares. Data output is available on the falling edge of each clock pulse. DOUT goes into a high-impedance state as soon as $\overline{CS}$ is pulled high.

Table 5 and Table 6 show the formats of the write and read words, respectively. As shown in Table 5, some of the bits written to the SPI register are ignored and can be set to either 0 or 1. The bit description table (Table 7)

describes each bit in the data input and output and indicates whether it is a read-only or read/write bit.

Enable

When ENP is pulled high with EN1 and EN2 low, the device allows SPI to independently enable and disable each switching and linear regulator.

Status and Power-Good Indicators

A number of status-monitoring circuits detect and indicate irregular conditions. The SPI output data includes information about the device thermal shutdown status and undervoltage conditions on the switching and linear regulator outputs.

Specifically, flags are set to indicate if the device junction temperature exceeds +165°C and if the output voltages of the switching and linear regulators fall below 85% of their set values.

Soft-Start

The soft-start time of the linear regulators, defined as the amount of time it takes for the regulator output to ramp from 0V to the set voltage, is programmable between 6.78ms, 13.6ms, 27.1ms, and 54.3ms.

Current Limit (Boost and Cuk)

The current limit (I_{LIM}) of the switching converters is programmable based on Table 1.

Current Limit During Soft-Start

The current limit of the switching converters during soft-start is programmable based on Table 1. After the soft-start period, the current limit is reset to the programmed current limit.

VCOM DAC

An integrated 7-bit DAC provides offset to the VCINH and VCINL inputs in increments of 7.8mV in a positive direction. The size of the offset is given as:

VCOM Offset = N x 7.8mV

where N is the numeric value of the digital code stored in DAC[6:0]. Table 4 shows the relationship of the VCOM DAC offset and selected digital codes.

Table 4. VCOM DAC Offset

SPI CONTROL BITS FOR DAC		VCOM DAC OFFSET (mV)
DACU	DAC[6:0]	
1	111 1111	+998.4
1	100 0000	+499.2
1	000 0000	0

Table 5. Write Format (R/$\overline{W}$ = 0)

BIT NAME	R/$\overline{W}$	—	—	—	—	ENVSLS	ENVSH	VSHLIM1	VSHLIM0	VSHLIM66	—	ENVSL	VSLLIM1	VSLLIM0	VSLLIM66	—	ENVGH	VGHSTTI1	VGHSTTI0	—	ENVGL	VGLSTTI1	VGLSTTI0	—	DACU	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: *"—" is ignored by the SPI register and can be set to either 0 or 1.*

Table 6. Read Format (R/$\overline{W}$ = 1)

BIT NAME	X	VSLS_ON	T	VCOMH	VCOML	PGVSH	ENVSH	VSHLIM1	VSHLIM0	VSHLIM66	PGVSL	ENVSL	VSLLIM1	VSLLIM0	VSLLIM66	PGVGH	ENVGH	VGHSTTI1	VGHSTTI0	PGVGL	ENVGL	VGLSTTI1	VGLSTTI0	PGVIN	DACU	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: *"X" reflects the R/$\overline{W}$ bit from the previous write sequence.*

Table 7. Bit Description

BIT NUMBER	BIT NAME	READ/ WRITE	FUNCTION
31	R/$\overline{W}$	W	0 = Write to the SPI register and read out the current contents. 1 = Read out the contents of the SPI register. The remaining 31 bits are don't cares and are not written to the register.
30	VSLS_ON	R	VSL Switch Status: 0 = VSL switch is off. 1 = VSL switch is on.
29	T	R	Thermal-Shutdown Indicator: 0 = Die temperature is not over +165°C. 1 = Die temperature exceeds +165°C.
28	VCOMH	R	Positive VCOM Buffer Status: 0 = Positive VCOM buffer is inactive. 1 = Positive VCOM buffer is active.
27	VCOML	R	Negative VCOM Buffer Status: 0 = Negative VCOM buffer is inactive. 1 = Negative VCOM buffer is active.
26	PGVSH	R	VSH Boost Converter Power-Good Indicator: 0 = VSH is out of regulation. 1 = VSH is within regulation.
	ENVSLS	W	VSL Switch Enable: 0 = Turn off VSL switch. 1 = Turn on VSL switch.
25	ENVSH	R/W	Boost Converter Enable: 0 = Disable the converter (default). 1 = Enable converter.
24	VSHLIM1	R/W	Boost Converter Current Limit: 00 = See Table 1 and the current-limit equation. 01 = See Table 1 and the current-limit equation. 10 = See Table 1 and the current-limit equation. 11 = See Table 1 and the current-limit equation.
23	VSHLIM0	R/W	
22	VSHLIM66	R/W	Boost Converter Startup Current Limit: 0 = Set the current limit during startup to I_{LIM} (default). 1 = Reduce the current limit during soft-start.
21	PGVSL	R	VSL Cuk Converter Power-Good Indicator: 0 = VSL is out of regulation. 1 = VSL is within regulation.
20	ENVSL	R/W	Cuk Converter Enable: 0 = Disable the converter (default). 1 = Enable converter.
19	VSLLIM1	R/W	Cuk Converter Current Limit: 00 = See Table 1 and the current-limit equation. 01 = See Table 1 and the current-limit equation. 10 = See Table 1 and the current-limit equation. 11 = See Table 1 and the current-limit equation.
18	VSLLIM0		

Table 7. Bit Description (continued)

BIT NUMBER	BIT NAME	READ/ WRITE	FUNCTION
17	VSLLIM66	R/W	Cuk Converter Startup Current Limit: 0 = Set the current limit during startup to I_{LIM} (default). 1 = Reduce the current limit during soft-start.
16	PGVGH	R	VGH Positive Voltage-Linear Regulator Power-Good Indicator: 0 = VGH is out of regulation. 1 = VGH is within regulation.
15	ENVGH	R/W	VGH Positive Voltage-Linear Regulator Enable: 0 = Disable the regulator (default). 1 = Enable the regulator.
14	VGHSTTI1	R/W	VGH Linear Regulator Soft-Start Timing: 00 = Set the soft-start time to 6.78ms (default). 10 = Set the soft-start time to 13.6ms. 01 = Set the soft-start time to 27.1ms. 11 = Set the soft-start time to 54.3ms.
13	VGHSTTI0	R/W	
12	PGVGL	R	VGL Negative Voltage-Linear Regulator Power-Good Indicator: 0 = VGL is out of regulation. 1 = VGL is within regulation.
11	ENVGL	R/W	VGL Negative Voltage-Linear Regulator Enable: 0 = Disable the regulator (default). 1 = Enable the regulator.
10	VGLSTTI1	R/W	VGL Linear Regulator Soft-Start Timing: 00 = Set the soft-start time to 6.78ms (default). 10 = Set the soft-start time to 13.6ms. 01 = Set the soft-start time to 27.1ms. 11 = Set the soft-start time to 54.3ms.
9	VGLSTTI0		
8	PGVIN	R	INA Input Supply Power-Good Indicator: 0 = V_{INA} is below UVLO. 1 = V_{INA} is above UVLO.
7	DACU	R/W	Reserved bit: always set to 1.
6	DAC6	R/W	VCOM DAC Digital Input Bits. Use DAC[6:0] to adjust the VCOM DAC output from 0 to ±1V in 7.8mV increments. See the *VCOM DAC* section to determine the relationship between the output voltage and digital input.
5	DAC5	R/W	
4	DAC4	R/W	
3	DAC3	R/W	
2	DAC2	R/W	
1	DAC1	R/W	
0	DAC0	R/W	

Stand-Alone Mode

The device can be used in stand-alone mode without the SPI interface. When unused, connect the data and clock inputs, DIN and CLK, to GND. The chip-select input, $\overline{CS}$, is internally pulled up to INA and can either be left unconnected or connected to INA. In this mode, the default current-limit and soft-start values are used and sequencing is controlled using the EN1 and EN2 inputs as illustrated in Table 3. Since the DAC value cannot be changed, use the VCINH and VCINL inputs to set the VCOMH or VCOML output levels.

Design Procedure

Buck Converter

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). To determine the inductance value, select the ratio of inductor peak-to-peak AC current to DC average current (LIR) first. For LIR values that are too high, the RMS currents are high, and therefore I^2R losses are high. Use high-valued inductors to achieve low LIR values. Typically, inductance is proportional to resistance for a given package type, which again makes I^2R losses high for very low LIR values. A good compromise between size and loss is to select a 30% to 60% peak-to-peak ripple current to average-current ratio. If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR can increase between 0.5 and 1.0. The value of the inductor is determined as follows:

$$L = \frac{(V_{IN3} - V_{OUT3}) \times D}{LIR \times I_{OUT3} \times f_{SW}}$$

and:

$$D = \frac{V_{OUT3}}{\eta \times V_{IN3}}$$

where V_{IN3} is the input voltage, V_{OUT3} is the output voltage, I_{OUT3} is the output current, η is the efficiency of the buck converter, D is the duty cycle, and f_{SW} is 2.1MHz (the switching frequency of the buck converter). The efficiency of the buck converter can be estimated from the *Typical Operating Characteristics* and accounts for losses in the internal switch, catch diode, inductor R_{DC}, and capacitor ESR.

The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but also improve transient response and reduce efficiency due to higher peak currents. On the other hand, higher inductance increases efficiency by reducing the RMS current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The saturation current rating (I_{SAT}) must be high enough to ensure that saturation can occur only above the maximum current-limit value. If the buck output must withstand short-circuit conditions, an inductor with saturation current of 6A must be used.

Capacitor Selection

The input and output filter capacitors should be of a low ESR type (tantalum, ceramic, or low-ESR electrolytic) and should have IRMS ratings greater than:

$$I_{IN(RMS)} = I_O \sqrt{D \times (1\text{-}D + \frac{LIR^2}{12})}$$

for the input capacitor:

$$I_{OUT(RMS)} = \frac{LIR \times I_O}{\sqrt{12}}$$

for the output capacitor where D is the duty cycle given above.

The output voltage contains a ripple component whose peak-to-peak value depends on the value of the ESR and capacitance of the output capacitor, and is approximately given by:

$$\Delta V_{RIPPLE} = \Delta V_{ESR} + \Delta V_{CAP}$$

$$\Delta V_{ESR} = LIR \text{ x } I_O \text{ x } R_{ESR}$$

$$\Delta V_{CAP} = \frac{LIR \times I_O}{8 \times C \times f_{SW}}$$

Diode Selection

The catch diode should be a Schottky type to minimize its voltage drop and maximize efficiency. The diode must be capable of withstanding a reverse voltage of at least $V_{IN3(MAX)}$, the maximum value of the input voltage. The diode should have an average forward-current rating greater than:

$$ID = IO \text{ x } (1\text{-}D)$$

where D is the duty cycle given above. In addition, ensure that the peak-current rating of the diode is greater than:

$$I_{OUT} \times \left(1 + \frac{LIR}{2}\right)$$

Boost Converter

Inductor Selection

Considerations used in selecting an inductor for the buck converter are equally applicable in selecting an inductor for the boost converter. Use the following equations to determine an appropriate inductor value:

$$LP = \frac{V_{IN} \times D}{LIR \times I_{IN} \times f_{SW}}$$

and:

$$I_{IN} = \frac{V_O \times I_O}{\eta V_{IN}}$$

$$D = 1 - \frac{\eta V_{IN}}{V_O}$$

where V_{IN} is the input voltage, V_O is the output voltage, I_O is the output current, η is the efficiency of the boost converter, D is the duty cycle, and f_{SW} is 1.2MHz (the switching frequency of the boost converter). The efficiency of the boost converter can be estimated from the *Typical Operating Characteristics* and accounts for losses in the internal switch, catch diode, inductor R_{DC}, and capacitor ESR.

Capacitor Selection

The input and output filter capacitors should be of a low ESR type (tantalum, ceramic, or low-ESR electrolytic) and should have I_{RMS} ratings greater than:

$$I_{IN(RMS)} = \frac{LIR \times I_{IN}}{\sqrt{12}}$$

for the input capacitor:

$$I_{OUT(RMS)} = I_O \sqrt{\frac{D + \frac{LIR^2}{12}}{1 - D}}$$

for the output capacitor, where I_{IN} and D are the input current and duty cycle given above.

The output voltage contains a ripple component whose peak-to-peak value depends on the value of the ESR and capacitance of the output capacitor, and is approximately given by:

$$\Delta V_{RIPPLE} = \Delta V_{ESR} + \Delta V_{CAP}$$

$$\Delta V_{ESR} = I_{IN} \times (1 + \frac{LIR}{2}) \times R_{ESR}$$

$$\Delta V_{CAP} = \frac{I_O \times D}{C \times f_{SW}}$$

where I_{IN} and D are the input current and duty cycle given above.

Rectifier Diode

The catch diode should be a Schottky type to minimize its voltage drop and maximize efficiency. The diode must be capable of withstanding a reverse voltage of at least V_{VSH}. The diode should have an average forward current rating greater than:

$$I_D = I_{IN} \times (1 - D)$$

where I_{IN} and D are the input current and duty cycle given above. In addition, ensure that the peak-current rating of the diode is greater than:

$$I_{IN} \times \left(1 + \frac{LIR}{2}\right)$$

Output-Voltage Selection

The output voltage of the boost converter can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between the output and FBP and connect R_{BOTTOM} between FBP and GND. Select R_{BOTTOM} in the 10kΩ to 50kΩ range. Calculate R_{TOP} with the following equation:

$$R_{TOP} = R_{BOTTOM} \times (\frac{V_{VSH}}{V_{FBP}} - 1)$$

where V_{FBP}, the boost converter's feedback set point, is 1V. Place both resistors as close to the device as possible. Connect R_{BOTTOM} to the analog ground plane and route this connection away from the power traces.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator pole to maintain loop stability. For low-ESR output capacitors, use Table 8 to select initial values for R_{COMP} and C_{COMP}. Use a 15pF capacitor in parallel to R_{COMP} and C_{COMP}.

Table 8. Boost Example Compensation Values

V_{VSH} (V)	5	7	13	15
I_{VSH} (A)	0.6	0.6	0.1	0.3
P_{OUT} (W)	3	4.2	1.3	4.5
Inductor value (µH)	3.3	3.3	15	4.7
R_{COMP} (kΩ)	47	56	31	56
C_{COMP} (pF)	220	270	680	390

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms. The ideal transient response is achieved when the output settles quickly with little or no overshoot. Connect the compensation network to the analog ground plane and route this connection away from the power traces.

p-Channel FET Selection

The p-channel FET used to gate the boost-converter's input should have low on-resistance as it affects overall efficiency of the boost converter. The FET must be rated to the full current rating of boost inductor. Connect a resistor (R_{SG}) between the source and gate of the FET. Under normal operation, R_{SG} carries a gate drive current of 53µA (typ) and 36µA (min) and the resulting gate-source voltage (V_{GS}) turns on the FET. When the gate drive is removed under a fault condition or in shutdown, R_{SG} bleeds off charge to turn off the FET. Size R_{SG} to produce the V_{GS} needed to turn on the FET.

Cuk Converter

Inductor Selection

Considerations used in selecting an inductor for the buck converter are equally applicable in selecting an inductor for the Cuk converter. Use the same value and type of inductor for LN1 and LN2. Use the following equation to determine their value:

$$LN1 = LN2 = \frac{V_{INA} \times D}{LIR \times I_{IN} \times f_{SW}}$$

The input current and duty cycle are calculated as follows:

$$I_{IN} = \frac{|V_{VSL}| \times |I_O|}{\eta V_{INA}}$$

$$D = \frac{|V_{VSL}| + V_{SCHOTTKY}}{V_{INA} + |V_{VSL}| + V_{SCHOTTKY}}$$

In the equations above, V_{INA} is the input voltage, V_{VSL} is the output voltage, I_{IN} is the input current, I_O is the output current, η is the efficiency of the Cuk converter, D is the duty cycle, and f_{SW} is 1.2MHz (the switching frequency of the Cuk converter). The efficiency of the Cuk converter can be estimated from the *Typical Operating Characteristics* and accounts for losses in the internal switch, catch diode, inductor R_{DC}, and capacitor ESR.

Capacitor Selection

The value of the Cuk coupling capacitor, C_1, can be calculated as follows:

$$C_1 = \frac{|I_O| \times D}{CVR \times (V_{IN} + |V_{VSL}|) \times f_{SW}}$$

where CVR is the capacitor voltage-ripple ratio and is the ratio of the capacitor's voltage ripple to the average voltage across the coupling capacitor. A good starting value for CVR is 0.05. It is important that a low-ESR type is used as all the output power flows through this capacitor. The voltage rating of the coupling capacitor must be at least $V_{INA} + |V_{VSL}|$.

The input and output filter capacitors should be of a low-ESR type (tantalum, ceramic, or low-ESR electrolytic) and should have I_{RMS} ratings greater than:

$$I_{IN(RMS)} = \frac{LIR \times I_{IN}}{\sqrt{12}}$$

for the input capacitor:

$$I_{OUT(RMS)} = \frac{LIR \times |I_O|}{\sqrt{12}}$$

for the output capacitor, where I_{IN} is the input current given above.

The output voltage contains a ripple component whose peak-to-peak value depends on the value of the ESR and capacitance of the output capacitor, and is approximately given by:

$$\Delta V_{RIPPLE} = \Delta V_{ESR} + \Delta V_{CAP}$$

$$\Delta V_{ESR} = LIR \times |I_O| \times R_{ESR}$$

Rectifier Diode

The catch diode should be a Schottky type to minimize its voltage drop and maximize efficiency. The diode must be capable of withstanding a reverse voltage of at least ($V_{INA} + |V_{VSL}|$). The diode should have an average forward current rating greater than:

$$I_D = (I_{IN} + |I_O|) \times (1 - D)$$

where I_{IN} and D are the input current and duty cycle given above. In addition, ensure that the peak-current rating of the diode exceeds $I_{IN} + |I_O|$.

Output-Voltage Selection

The output voltage of the Cuk converter can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between REF and FBGL and connect R_{BOTTOM} between FBGL and the output of the Cuk converter. Select R_{TOP} greater than 20kΩ to avoid loading down the reference output. Calculate R_{BOTTOM} with the following equation:

$$R_{BOTTOM} = R_{TOP} \times \frac{V_{FBN} + |V_{VSL}|}{V_{REF} - V_{FBN}}$$

where V_{VSL} is the desired output voltage, V_{REF} = 1.25V, and V_{FBN} = 0.2 x V_{REF} = 0.25V (the regulated feedback voltage of the converter). Note that REF can only source up to 80µA total (for Cuk and VGL feedback).

Loop Compensation

See Table 9 to select the compensation components for the Cuk converter.

Selection of the n-Channel FET for VSL Output

An n-channel FET can be used to delay the on switch of the VSL output when the charge pumps use the VSL output voltage and VGH and/or VGL are required to be present before VSL (see Table 3 and specifically the mode for EN1 = EN2 = 1). The n-channel FET, connected in series with the Cuk converter's output, should have low on-resistance. Connect a resistor (R_{GS}) between the gate and source of the FET. Under normal operation, R_{GS} carries a gate-drive current of 50µA, typ (38µA min) and the resulting gate-source voltage (V_{GS}) turns on the FET. Size R_{GS} to produce the V_{GS} needed to turn on the FET.

When this FET is not used, leave VSLS unconnected.

Charge Pumps

Selecting the Number of Charge-Pump Stages

For most applications, a single-stage charge pump suffices as shown in the *Typical Operating Circuits*. The flying capacitor can be connected to either LXN or LXP. In the LXN case, the output voltages are:

$$V_{VCP} = V_{INA} + |V_{VSL}| + V_{SCHOTTKY} + V_{VSH} - 2 \times V_D$$

$$V_{VCN} = -(V_{INA} + 2 \times |V_{VSL}| + V_{SCHOTTKY} - 2 \times V_D)$$

In the LXP case, the output voltages are:

$$V_{VCP} = 2 \times V_{VSH} - V_{SCHOTTKY} - 2 \times V_D$$

$$V_{VCN} = -(|V_{VSL}| + V_{VSH} - V_{SCHOTTKY} - 2 \times V_D)$$

The equations above assume that the inverting charge pump is connected to the Cuk output (Figure 9). In the case where the Cuk converter is unused or operates in parallel with the boost converter, connect the inverting charge pump to ground (Figure 10), make LXP the switching node, use the equations for the LXP case, and set $|V_{VSL}|$ to 0V in those equations.

Table 9. Cuk Example Compensation Values

V_{VSL} (V)	-5	-7	-12
I_{VSL} (A)	+0.6	+0.6	+0.1
P_{OUT} (W)	+3	+4.2	+1.2
Inductor value (µH)	+3.3	+3.3	+15
R_{COMPN} (kΩ)	+47	+56	+31
C_{COMPN} (pF)	+220	+270	+680

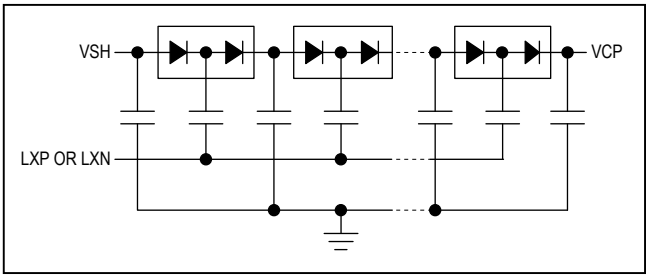


Figure 6. Multistage Noninverting Charge Pump for Positive Output (Cuk is Active; If Cuk is Inactive, Make LXP the Switching Node)

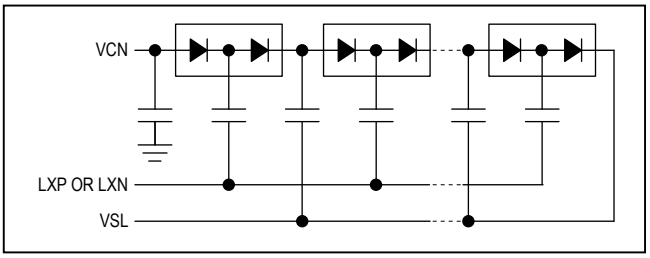


Figure 7. Multistage Inverting Charge Pump for Negative Output (Cuk is Active)

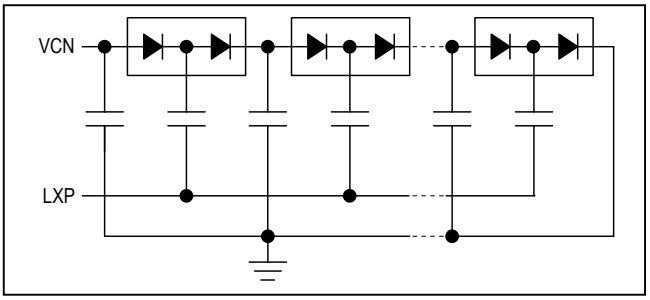


Figure 8. Multistage Inverting Charge Pump for Negative Output (Cuk is Inactive)

If larger output voltages are needed, use multistage charge pumps (however, the maximum charge-pump voltage is limited by the absolute maximum ratings of VCP and DRVN). Figure 6, Figure 7, and Figure 8 show the configuration of a multistage charge pump for both positive and negative outputs.

For multistage charge pumps with LXN as the switching node, the output voltages are given by:

$$V_{VCP} = n \times (V_{INA} + |V_{VSL}| + V_{SCHOTTKY} + V_{VSH} - 2 \times V_D)$$

$$V_{VCN} = -n \times (V_{INA} + 2 \times |V_{VSL}| + V_{SCHOTTKY} - 2 \times V_D)$$

For those with LXP as the switching node, the output voltages are:

$$V_{VCP} = n \times (2xV_{VSH} - V_{SCHOTTKY} - 2 \times V_D)$$

$$V_{VCN} = -n \times (|V_{VSL}| + V_{VSH} - V_{SCHOTTKY} - 2 \times V_D)$$

The equations above assume that the inverting charge pump is connected to the Cuk output (Figure 6 and Figure 7). In the case where the Cuk converter is unused or operates in parallel with the boost converter, connect the inverting charge pump to ground (Figure 8), make LXP the switching node, use the equations for the LXP case, and set $|V_{VSL}|$ to 0V in those equations.

Flying Capacitors

Increasing the flying-capacitor value lowers the effective source impedance and increases the output-current capability. However, increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The voltage rating of the flying capacitors for the noninverting charge pump should exceed V_{CP} while that for the negative-charge pump should exceed the magnitude of VCN.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output-ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required output capacitance for the noninverting charge pump connected to VCP:

$$C_{OUT\_VCP} \geq \frac{D \times I_{LOAD\_VCP}}{f_{SW} \times V_{RIPPLE\_VCP}}$$

where D is the duty cycle of the switching node to which the flying capacitor is connected, C_{OUT_VCP} is the output capacitor of the noninverting charge pump, I_{LOAD_VCP} is the load current of the noninverting charge pump, f_{SW} is the switching frequency of the boost and Cuk converters, and V_{RIPPLE_VCP} is the peak-to-peak value of the output ripple.

For the inverting charge pump connected to VCN, use the following equation to approximate the required output capacitance:

$$C_{OUT\_VCN} \geq \frac{(1\text{-}D) \times I_{LOAD\_VCN}}{f_{SW} \times V_{RIPPLE\_VCN}}$$

where D is the duty cycle of the switching node to which the flying capacitor is connected, C_{OUT_VCN} is the output capacitor of the inverting charge pump, I_{LOAD_VCN} is the load current of the inverting charge pump, f_{SW} is the switching frequency of the boost and Cuk converters, and V_{RIPPLE_VCN} is the peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diodes

Use high-speed silicon switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps to avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating.

Positive Gate-Voltage Linear Regulator

Output-Voltage Selection

The output voltage of the positive gate-voltage linear regulator can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between the output and FBGH and connect R_{BOTTOM} between FBGH and GND. Select R_{BOTTOM} in the 10kΩ to 50kΩ range. Calculate R_{TOP} with the following equation:

$$R_{TOP} = R_{BOTTOM} \times (\frac{V_{VGH}}{V_{FBGH}} - 1)$$

where V_{VGH} is the desired output voltage and V_{FBGH} = 1V (the regulated feedback voltage for the regulator). Place both resistors as close to the device as possible.

Avoid excessive power dissipation within the internal pMOS device of the linear regulator by paying attention to the voltage drop across the drain and source. The amount of power dissipation is given by:

$$P_{DISS} = (V_{VCP} - V_{VGH}) \times I_{LOAD(MAX)}$$

where V_{VCP} is the noninverting charge-pump output voltage applied to the drain, V_{VGH} is the regulated output voltage, as well as the source voltage, and $I_{LOAD(MAX)}$ is the maximum load current.

Stability Requirements

The positive gate-voltage linear regulator (VGH) requires a minimum output capacitance for stability. For an output voltage of 5V to 22V and an output current of 10mA to 15mA, use a minimum capacitance of 0.47µF.

Negative Gate-Voltage Linear-Regulator Controller

Output-Voltage Selection

The output voltage of the negative gate-voltage linear regulator can be adjusted by using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between REF and FBGL and connect R_{BOTTOM} between FBGL and the collector of the external npn transistor. Select R_{TOP} greater than 20kΩ to avoid loading down the reference output: Calculate R_{BOTTOM} with the following equation:

$$R_{BOTTOM} = R_{TOP} \times \frac{V_{FBGL} - V_{VGL}}{V_{REF} - V_{FBGL}}$$

where V_{VGL} is the desired output voltage, V_{REF} = 1.25V, and V_{FBGL} = 0.25V (the regulated feedback voltage of the regulator).

Pass Transistor Selection

The pass transistor must meet specifications for current gain (h_{FE}), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = (I_{DRVN} - \frac{V_{BE}}{R_{BE}}) \times h_{FE(MIN)}$$

where I_{DRVN} is the minimum guaranteed base-drive current, V_{BE} is the transistor's base-to-emitter forward-voltage drop, and R_{BE} is the pulldown resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the ***Stability Requirements*** section), so excessive gain destabilizes the output.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator can support. Also, the package's power dissipation limits the usable maximum input-to-output voltage differential. The maximum power-dissipation capability of the transistor's package and mounting must exceed the actual power dissipated in the device. The power dissipated equals the maximum load current ($I_{LOAD(MAX)\_LR}$) multiplied by the maximum input-to-output voltage differential:

$$P_{DISS} = (V_{VGL} - V_{VCN}) \times I_{LOAD(MAX)}$$

where V_{VGL} is the regulated output voltage on the collector of the transistor, V_{VCN} is the inverting charge-pump output voltage applied to the emitter of the transistor, and $I_{LOAD(MAX)}$ is the maximum load current.

Stability Requirements

The VGL linear-regulator controller uses an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V\_LR} \cong (\frac{4}{V_T}) \times (1 + \frac{I_{BIAS} \times h_{FE}}{I_{LOAD}}) \times V_{REF}$$

where V_T is 26mV at room temperature, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). For the device, the bias current for the negative voltage-linear regulator is 0.1mA. Therefore, the base-to-emitter resistor should be chosen to set 0.1mA bias current:

$$R_{BE} = \frac{V_{BE}}{0.1mA} = \frac{0.7V}{0.1mA} = 6.8k\Omega$$

The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system, and the output capacitor's ESR generates a zero. For proper operation, use the following equations to verify the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE\_LR} = \frac{I_{LOAD(MAX)\_LR}}{2\pi \times C_{OUT\_LR} \times V_{OUT\_LR}}$$

The unity-gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V\_LR} \times f_{POLE\_LR}$$

2) The pole created by the internal amplifier delay is approximately 1MHz:

$$f_{POLE\_AMP} = 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance, the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times (R_{BE} // R_{IN})}$$

where:

$$C_{IN} = \frac{g_m}{2\pi f_T},\ R_{IN} = \frac{h_{FE}}{g_m}$$

g_m is the transconductance of the pass transistor, and f_T is the transition frequency. Both parameters can be found in the transistor's data sheet. Because R_{BE} is much greater than R_{IN}, the above equation can be simplified:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times R_{IN}}$$

Substituting for C_{IN} and R_{IN} yields:

$$f_{POLE} = \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the linear regulator's feedback resistance and the capacitance between FB and AGND (including stray capacitance):

$$f_{POLE\_FB} = \frac{1}{2\pi \times C_{FB} \times (R_{TOP} // R_{BOTTOM})}$$

where C_{FB} is the capacitance between FBGL node and GND (approximately 30pF), R_{TOP} is the upper resistor of the linear regulator's feedback divider, and R_{BOTTOM} is the lower resistor of the divider.

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{ZERO\_ESR} = \frac{1}{2\pi \times C_{OUT\_LR} \times R_{ESR}}$$

where R_{ESR} is the ESR of C_{OUT_LR}. To ensure stability, make C_{OUT_LR} large enough so the crossover occurs well before the poles and zero calculated in steps 2 to 5. The poles in steps 3 and 4 generally occur at several megahertz, and using ceramic capacitors ensures the ESR zero occurs at several megahertz as well. Placing the crossover below 500kHz is sufficient to avoid the amplifier-delay pole and generally works well, unless unusual component choices or extra capacitances move one of the other poles or the zero below 1MHz.

Table 10. Minimum Output Capacitance vs. Output Voltage Range for VGL Linear Regulator (I_{OUT} = 10mA to 15mA)

OUTPUT VOLTAGE RANGE (V)	MINIMUM OUTPUT CAPACITANCE (µF)
$-2 \geq V_{VGL} \geq -4$	2.2
$-5 \geq V_{VGL} \geq -7$	1.5
$-8 \geq V_{VGL} \geq -13$	1

Table 10 is a list of recommended minimum output capacitances for the VGL linear regulator and are applicable for output currents in the 10mA to 15mA range.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the buck converter, boost converter, Cuk converter, VGH linear regulator, VGL linear regulator controller, and the power dissipated by the VCOM buffers.

Buck Converter

In the buck converter, conduction and switching losses in the internal MOSFET are dominant. Estimate these losses using the following formula:

$$P_{LX3} \approx \left[(I_{IN(DC,\ MAX)} \times \sqrt{D})^2 \times R_{DS\_ON} \right] + \left[0.5 \times V_{IN3} \times I_{IN(DC,MAX)} \times (t_R + t_F) \times f_{SW} \right]$$

where R_{DS_ON} is the on-resistance of the buck converter's internal FET, t_R = 5ns, t_F = 5ns, and f_{SW} = 2.1MHz.

Boost Converter

In the boost converter, conduction and switching losses in the internal MOSFET are dominant. Estimate these losses using the following formula:

$$P_{LXP} \approx \left[(I_{IN(DC,MAX)} \times \sqrt{D})^2 \times R_{DS\_ON} \right] + \left[0.5 \times V_{VSH} \times I_{IN(DC,MAX)} \times (t_R + t_F) \times f_{SW} \right]$$

where R_{DS_ON} is on-resistance of the boost converter's internal FET, t_R = 7ns, t_F = 16ns, and f_{SW} = 1.2MHz.

Cuk Converter

A similar analysis applies to the Cuk converter. The power dissipation in the integrated low-side FET is:

$$P_{LXN} \approx \left[(I_{IN(DC,MAX)} \times \sqrt{D})^2 \times R_{DS\_ON} \right] + \left[(0.5 \times |V_{VSL}| + V_{INA}) \times I_{IN(DC,MAX)} \times (t_R + t_F) \times f_{SW} \right]$$

where R_{DS_ON} is on-resistance of the boost converter's internal FET, t_R = 7ns, t_F = 16ns, and f_{SW} = 1.2MHz.

Positive Gate-Voltage Linear Regulator

Use the lowest number of charge-pump stages possible in supplying power to the positive-voltage linear regulator. Doing so minimizes the drain-source voltage of the integrated pMOS switch and power dissipation. The power dissipated in the switch is given as:

$$P_{VGH} = (V_{VCP} - V_{VGH}) \times I_{LOAD(MAX)}$$

Negative Gate-Voltage Linear-Regulator Controller

Use the lowest number of charge-pump states possible to provide the negative voltage to the VGL linear regulator. Estimate the power dissipated in the VGL linear-regulator controller using the following:

$$P_{VGL} = (V_{INA} + |V_{VCN}| - V_{BE}) \times I_{DRVN}$$

where V_{BE} is the base-emitter voltage of the external npn bipolar transistor and I_{DRVN} is the current sourced from DRVN to the R_{BE} bias resistor and to the base of the transistor.

VCOM Buffers

The power dissipated in the VCOM buffers depends on the output current, the output voltage, and the supply voltages. The two VCOM buffers, VCOMH and VCOML, use separate supply rails. VCOMH is powered between VCOMP and GND while VCOML is powered between INA and VCOMN. The power dissipated in VCOMH is given by:

$$P_{VCOMH(SOURCE)} = (V_{VCOMP} - V_{COMH}) \times I_{OUT\_SOURCE}$$

$$P_{VCOMH(SINK)} = V_{COMH} \times I_{OUT\_SINK}$$

where I_{OUT_SOURCE} is the output current sourced by the buffer and I_{OUT_SINK} is the output current that the buffer sinks. Similarly, the power dissipated in the VCOML buffer is given by:

$$P_{VCOML(SOURCE)} = (V_{INA} - V_{COML}) \times I_{OUT\_SOURCE}$$

$$P_{VCOML(SINK)} = (V_{COML} - V_{VCOMN}) \times I_{OUT\_SINK}$$

Total Power Dissipation

The total power dissipated in the package is the sum of the losses calculated above and the power due to the quiescent current consumed in the device (I_{IN3} in continuous mode for the buck converter and I_{INA} for the rest of the device). Therefore, total power dissipation can be estimated as follows:

$$P_T = P_{LX3} + P_{LXP} + P_{LXN} + P_{VGH} + P_{VGL} + P_{VCOMH} + P_{VCOML} + (V_{IN3} \times I_{IN3}) + (V_{INA} \times I_{INA})$$

Achieve maximum heat transfer by connecting the exposed pad to a thermal landing pad and connecting the thermal landing pad to a large ground plane through thermal vias.

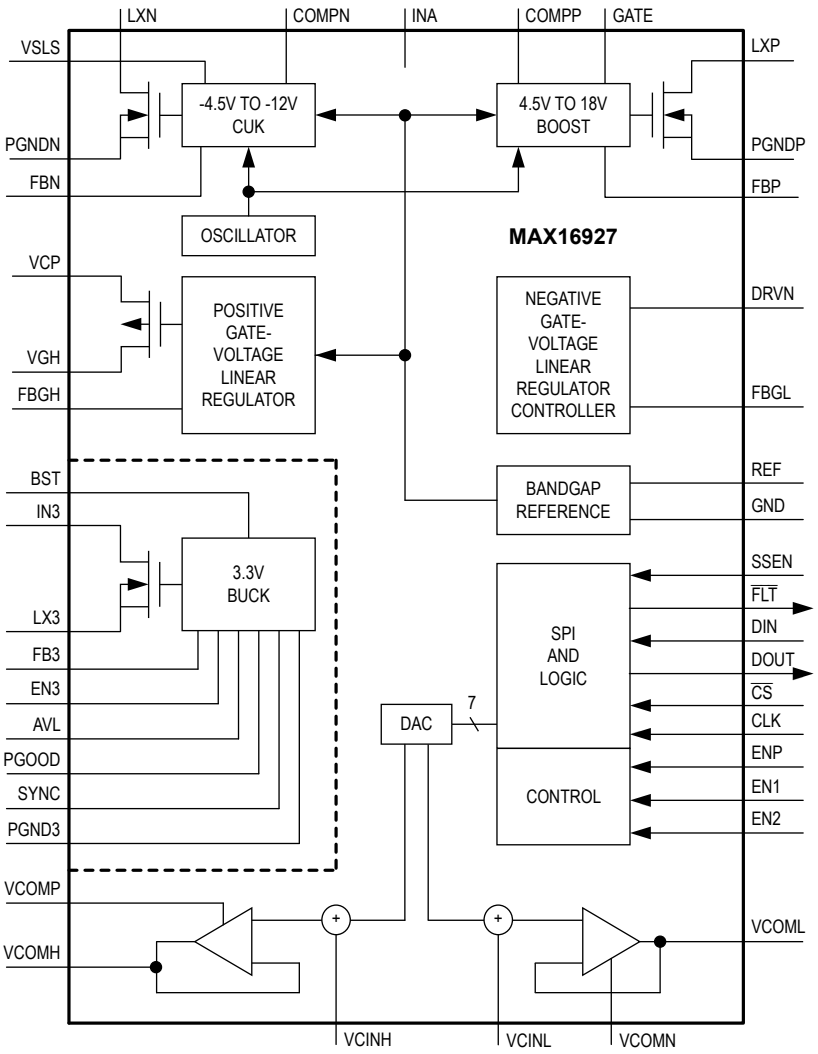
Layout Considerations

Careful PCB layout is critical in achieving stable and optimized performance. Follow the following guidelines for good PCB layout:

- Place decoupling capacitors as close to the IC as possible. Connect the power ground planes and the analog ground plane together at one point close to the device.
- Connect input and output capacitors to the power ground planes; connect all other capacitors to the signal ground plane.
- Keep the high-current paths as short and wide as possible. Keep the path of switching currents short.
- Place the feedback resistors as close to the IC as possible. Connect the negative end of the resistive divider, as well as compensation RC, to the analog ground plane and keep the center tap away from switching nodes.
- Route digital I/Os and high-speed switching nodes (LX3, LXN, and LXP) away from sensitive analog nodes (FB3, FBP, FBN, COMPP, COMPN, and REF).

Refer to the MAX16927 Evaluation Kit data sheet for a recommended PCB layout.

Block Diagram



Typical Operating Circuits

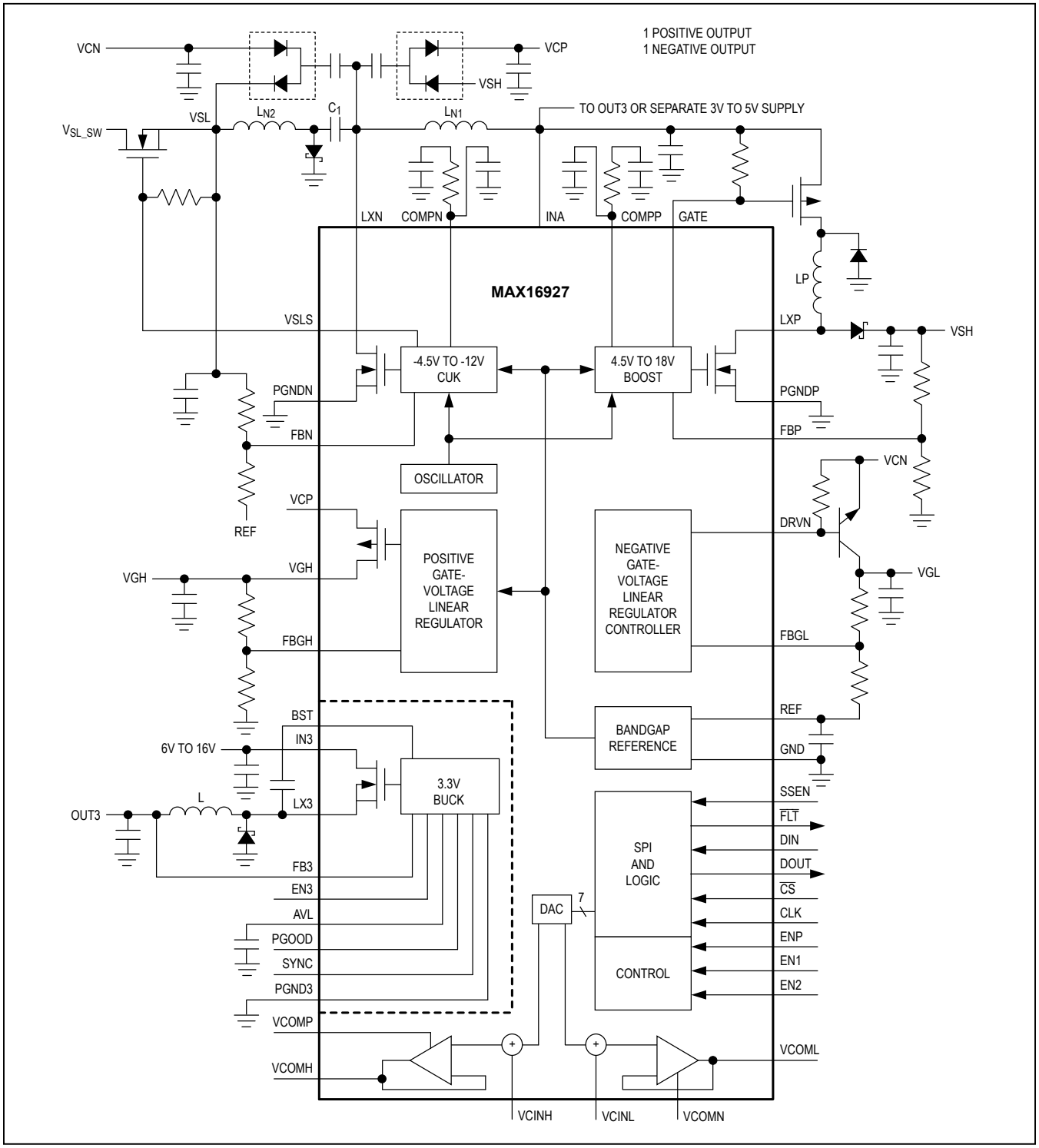


Figure 9. Typical Operating Circuit

Typical Operating Circuits (continued)

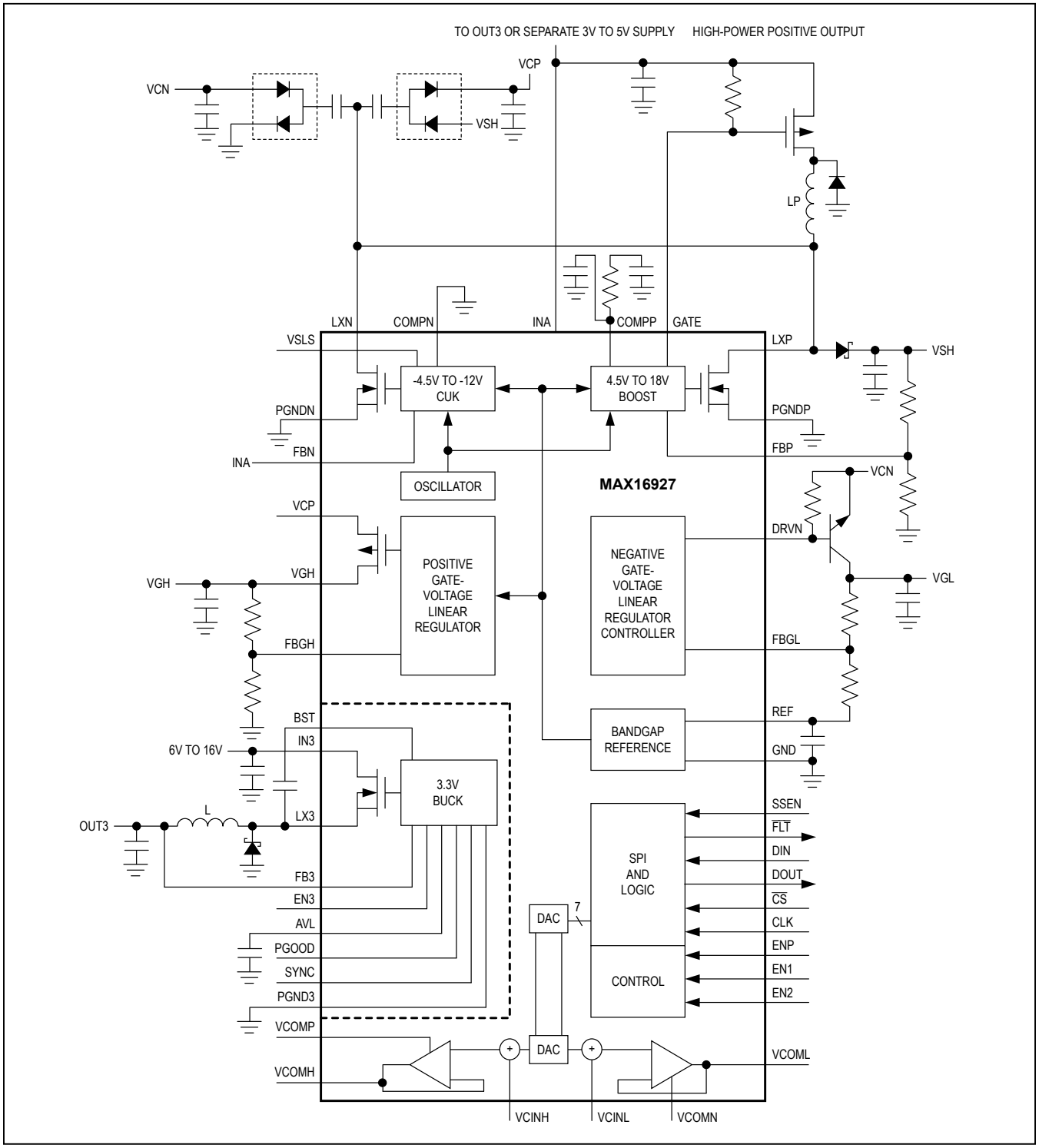


Figure 10. Typical High-Power Operating Circuit

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+7	21-0144	90-0133

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	12/10	Added “Measurement Bandwidth = 1kHz” to TOC 11 and TOC 12	9
2	9/13	Removed short INA to ENP, added description on how to enable boost converter, clarified INA > 2.9V then EN from low to go high	14, 19
3	10/14	Updated ***General Description***, ***Benefits and Features***, ***Pin Description***, ***VCOM Buffers***, ***VCOM DAC*** sections, and TOC 32, Table 4, and Table 7 to match VCOML buffer performance, and updated VGH and VGL soft-start time	1, 5, 12, 14, 19, 21, 23
4	1/18	Updated FBP regulation voltage in ***Electrical Characteristics*** table	4
5	4/18	Updated ***Output-Voltage Selection*** section	29
6	5/18	Updated 1st–4th supply sequence order for rows 5 and 6 in Table 3	20

