PIC18F6623/6723/8623/8723 Rev. B1 Silicon Errata

The PIC18F6623/6723/8623/8723 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS39894**B**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6623/6723/8623/8723 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F6623/6723/8623/8723 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6623	0100 1001 110	0 0010
PIC18F6723	0100 1010 000	0 0010
PIC18F8623	0100 1001 111	0 0010
PIC18F8723	0100 1010 001	0 0010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F6623/6723/8623/8723 silicon.

1. Module: Master Synchronous Serial Port (MSSP) – Serial Peripheral Interface (SPI)

In SPI mode, the Buffer Full flag (BF bit in the SSPxSTAT register), the Write Collision Detect bit (WCOL in SSPxCON1) and the Receive Overflow Indicator bit (SSPOV in SSPxCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set), and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPxBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus, clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Capture/Compare/PWM (CCP)

PWM output of 10-bit resolution is not available for either CCP4 or CCP5 when Timer4 is being used as the PWM time base (T3CON<6,3> = 01, 10 or 11) for the PWM mode (CCPxCON<3:2> = 11).

Work around

For 10-bit resolution, use Timer2 as the PWM time base (T3CON<6,3> = 00).

For 8-bit resolution, use Timer4 or Timer2 as the PWM time base and set the two LSBs to '00' (CCPxCON<5:4> = 00).

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP (I^2C™ Slave)

In extremely rare cases, when configured for I^2C™ slave reception, the MSSP module may not receive the correct data. This occurs only if the Serial Receive/Transmit Buffer (SSPxBUF) register is not read within a window after the SSPxIF interrupt has occurred.

For SSP1BUF, the flag bit is SSP1IF (PIR1<3>).

For SSP2BUF, the flag bit is SSP2IF (PIR3<7>).

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSP1CON2<0>).

- Each time the SSPxIF bit is set, read the SSPxBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: MSSP (I^2C™ Master)

If the module is in I^2C Master mode and the slave performs clock stretching, the first clock pulse after the slave releases the SCL line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/reception.

Work around

If the module is in I^2C Master mode, do not have the slave perform clock stretching. Alternately, the master can slow down the SCL clock frequency to a level where the slave can detect the narrowed clock pulse.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Enhanced Universal Synchronous Asynchronous (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN (RCSTAx <7>) bit = 0)
- The EUSART is re-enabled (RCSTAx <7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2-TCY delay after re-enabling the EUSART.

1. Disable the receive interrupts:
   - For RCSTA1 – RC1IE bit (PIE1<5>) = 0
   - For RCSTA2 – RC2IE bit (PIE3<5>) = 0
2. Disable the EUSART:
   - For RCSTA1 – SPEN bit (RCSTA1<7>) = 0
   - For RCSTA2 – SPEN bit (RCSTA2<7>) = 0
3. Re-enable the EUSART (RCSTAx <7> = 1). (See Step 1.)
4. Re-enable the receive interrupts:
   - For RCSTA1 – RC1IE bit (PIE1<5>) = 1
   - For RCSTA2 – RC2IE bit (PIE3<5>) = 1

   (This is the first TCY delay.)
5. Execute a NOP instruction.

   (This is the second TCY delay.)

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Timer1

When Timer1 is running on the Timer1 oscillator, if Sleep mode is executed immediately after loading Timer 1 with 0xFFFF, the Timer1 interrupt will not get set on the first overflow from 0xFFFF to 0x0000.

All subsequent overflows, from 0xFFFF to 0x0000, will work correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (8/2007)

Initial release of this errata. Includes silicon issues 1 (MSSP) and 2 (CCP).

Rev B Document (9/2010)

Added silicon issues 3 MSSP (I^2C™ Slave), 4 (MSSP I^2C™ Master), 5 Enhanced Universal Synchronous Asynchronous (EUSART) and 6 (Timer1).

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